ESD Myths and the Latency Controversy

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Understanding some common myths about ESD can help manufacturers build successful ESD programs.

There are a number of common misunderstandings and controversies about electrostatic discharge (ESD) program management that can have significant impact on the implementation and maintenance of an ESD program. Some of these misunderstandings or myths result in unnecessary expenditures, whereas others result in a compromise of the program integrity. Skeptics not wanting to adhere to certain standard ESD procedures often cite the myths and controversies, such as latency. Consequently, it is important to identify and dispel the myths, as well as to understand the potential effect of latent failures.

This article outlines 5 of the 15 most common myths (see sidebar on page 114). Three supporting case studies are provided, including a case study on latency. The remaining myths and several additional case studies are discussed in *ESD Program Management*.[1] The myths and case studies presented here were chosen to provide real-world examples of how an ESD program can be strengthened by understanding the fallacy in each myth. This understanding will result in more-reliable products that are also more cost-competitive.

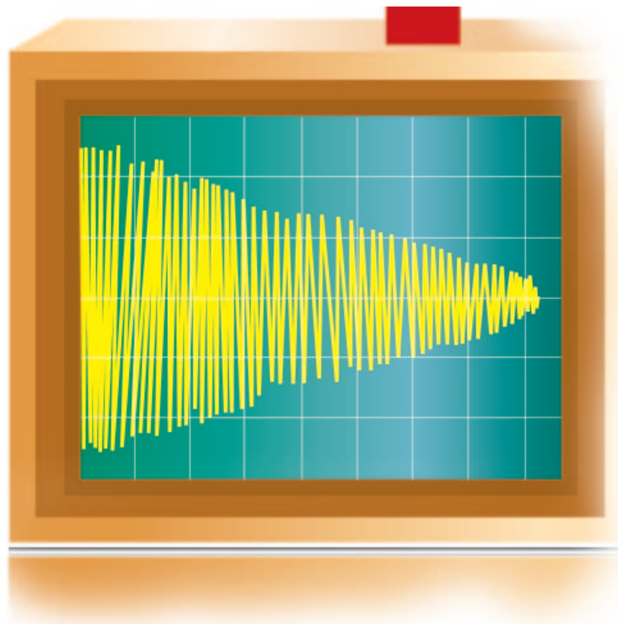

Illustration by TAISHA PAYTON

Although not a myth, latency is a significant reliability consideration that is surrounded with controversy. Some experts argue that latency is virtually nonexistent, and others claim that it is the dominant failure mode. Reality lies somewhere in between. The third case study cites irrefutable evidence of latent failures in alarming proportions that must be factored into sound ESD program management and product design.

Common Myths

Myth 2: PWB Assemblies Are Not ESD Sensitive. Many individuals believe that once a component is inserted into a printed wiring board (PWB) assembly, the component is no longer ESD sensitive.

Truth. The ESD failure rate and sensitivity of a component can increase after it is inserted into a PWB assembly. One reason for this occurrence is that sensitive device junctions may become more easily accessible through the conductor paths of the PWB assemblies. Furthermore, laboratory tests have quantified this phenomenon.

In one test, the withstand voltage of a sensitive bipolar component was determined to have increased by only 20% (which is considered virtually no increase) when the component was tested in a PWB assembly. Even a metal shunt on the edge connector of this assembly had little impact on the sensitivity of the component. Therefore, the component was equally sensitive on or off of the PWB assembly.

At the very least, ESD controls are as important for PWB assemblies as they are for components. For instance, Case Studies 1 and 2 cite instances in which significant device failure rates developed at the circuit-board level.

Myth 3: One ESD Sensitivity Classification Is Sufficient for All Areas. Many companies view multiple work-area classifications as unnecessary and cumbersome. These companies arbitrarily assign the same classification to all ESD-sensitive components or assemblies. As a consequence, they lose the opportunity to maximize both the flexibility and the cost-effectiveness of the program.

Truth. All components are not the same. For example, the differences between the control practices for Class 0 and Class I components can be dramatic. Class 0 devices often require extraordinary precautions that are impracticable for general

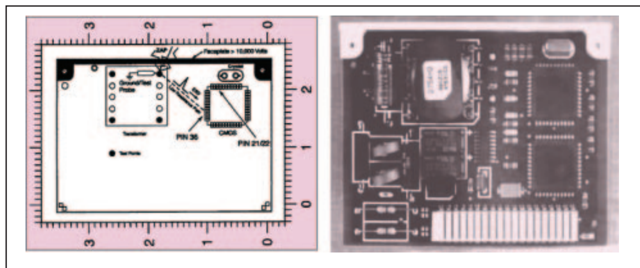

Figure 1. Schematic and photo of a circuit pack with plastic faceplate.

application, cost-prohibitive, and not defined in industry standards. It is a cost-effective and common practice, on the other hand, for standard Class I ESD procedures to be applied across the majority of product lines while reserving the extraordinary precautions for Class 0 devices.

In some applications, even greater granularity for older, less-sensitive products may be cost-effective. Therefore, companies manufacturing a diverse range of products may benefit from multiple classifications and need at least two classifications (Class 0 and Class I). Even if Class 0 products are not currently in production, it is essential to anticipate the possibility.

In doing so, companies can use less-expensive measures for older, less-sensitive technologies and reserve more-costly program parameters for only those manufacturing areas that require them, such as those for Class 0. The secret to implementing multiple classifications successfully is to do it so that training is virtually the same for all employees. Engineering provides the appropriate ESD control tools based on sensitivity, and employees are trained to use all tools with the same techniques. Generally, the classification is based on the most-sensitive component in the area.

In summary, companies must adopt a minimum of two area classifications—even if it is simply to anticipate the possibility of introducing Class 0 devices and the extraordinary precautions they require. Acknowledging Class 0 often leads to beneficial policy changes.

Myth 4: Human Body Model (HBM) Data Are Sufficient for Detecting Device Sensitivity Levels.

Truth. Companies that rely solely on HBM data fail to recognize the importance of charged-device-model (CDM) data. Because HBM was the first model developed, the most readily available data are HBM, and the vast majority of programs are based on HBM thresholds. As a result, HBM countermeasures have become widely used and highly effective.

However, CDM failures are now far more prevalent in factories because it is almost impossible to prevent components and assemblies from becoming charged. This prevalence is especially of concern because of the high-throughput automated assembly and test equipment used in most factories. Therefore, CDM data and mitigation techniques are vital to any ESD program.[2] Industry standards for CDM simulation are still being refined; however, integrated circuit (IC) suppliers are generally performing the tests on new designs. Regardless of the evolution of simulation standards, CDM mitigation techniques are an essential element in an ESD program and are strongly recommended. For instance, it is critically important to be aware of any Class 0 CDM devices prior to production.

For example, at the Lucent Technologies facility in North Andover, MA, diligent failure-mode analysis (FMA) conducted by quality assurance failed to reveal any HBM failures during the past 15 years. On the other hand, CDM failures continued to occur on occasion. These failures are understandable because CDM mitigation techniques are significantly more complicated and not as well understood as HBM techniques. Failure-mode laboratories at major IC suppliers have reported that the vast majority of their ESD field returns and device failures are CDM damage and not HBM or machine model (MM). This majority is caused in part by the fact that the vast majority of opportunities for ESD damage in the workplace are CDM related.

It should also be noted that some companies do not fully understand the relevance of the MM. MM is a variation of HBM and does not provide a reliable simulation of ESD damage caused by machines. MM typically produces failures that are very similar to HBM, but with a failure threshold voltage approximately 10 to 20 times lower. For example, a device with an HBM threshold of 800 V is likely to have an MM threshold of 40–80 V.

Numerous reports have documented this strong correlation between HBM and MM. Japan has downgraded the MM standard to an advisory. Other standards bodies are considering similar action. IC suppliers, in recent years, have begun to conduct CDM tests routinely and to design CDM protection into the components. Because of cost implications and diminishing requests for the data, MM, on the other hand, is often done on request only. As a result, the MM data have little value in developing and implementing an ESD program. These data often prompt companies to overreact, because MM thresholds are extraordinarily low. However, MM is a useful tool for FMA.

In summary, a sound ESD program must be developed and maintained on the basis of both HBM and CDM device testing and handling-mitigation techniques. It would be impractical to retrieve data on all existing products, but it is strongly recommended to seek the CDM data on new designs and as part of any FMA activities.

MM can also be useful as a diagnostic tool. It should be noted that estimating CDM failure thresholds is virtually impossible and that there is no correlation between HBM and CDM. As previously stated, it is critically important to be aware of any Class 0 components for either HBM or CDM prior to production.

Myth 8: Grounded Metal Is a Safe Surface for ESD-Sensitive Components or Assemblies.

Truth. Conductive materials are not safe surfaces for components that may be charged. This is true regardless of whether the conductive material is grounded. The CDM event occurs rapidly between two objects, and the resistance to ground (including a 1-MΩ resistor) has virtually no impact.

Myth 9: Designed-in ESD Protection Precludes the Need for ESD-Handling Controls.

Truth. Although designed-in protection generally improves the withstand voltage of components and PWB assemblies, this protection has technological limits. Total immunity is nearly impossible to achieve without an enclosure. Trade-offs

between performance and designed-in protection are very common. As a result, a sound ESD program requires a combination of good design and sound manufacturing practices.

Case Studies

Case Study 1: ESD (Field-Induced CDM) Caused by Charged Plastic Faceplate. This case study illustrates the fallacy explained in four of the myths. The high failure rates cited below occurred to circuit boards in spite of the premise in Myth 2: PWB Assemblies Are Not ESD Sensitive. The failures were also CDM rather than HBM, which indicates that CDM data are necessary for sound program development (Myth 4). Grounded metal test probes triggered the damaging CDM transients (Myth 8), clearly indicating that a grounded metal surface is not ESD safe for charged products. Finally, the designed-in protection (1500 V) of the component exceeded design requirements, but was still insufficient to prevent damage from occurring (Myth 9). Therefore, both designed-in protection and sound handling practices are essential safeguards.

A recent experience in one factory pointed out that the root cause of ESD problems can be very simple. Many printed wiring assemblies (circuit packs) include a cover or faceplate that provides a protective covering when the pack is installed in a shelf (see Figure 1).

In many designs, these faceplates are metallic and grounded to provide good electromagnetic compatibility (EMC). However, to keep material costs down, they are often made of insulating plastic. EMC design issues are then addressed using other techniques.

In this case, a system was designed using plastic faceplates. The system was in low-level production for more than a year without any indication of a significant problem. However, at one point, the removal rate of a certain linear complementary metal-oxide semiconductor (CMOS) part began to rise. The rate averaged 2.5%, with rates as high as 40% on certain days. The device failures were observed after the circuit-pack test, and the observed electrical signature was excessive leakage current between two pins on the device. The leakage was high enough to cause the circuit pack to fail its functional requirements.

These observations and subsequent FMA pointed strongly to ESD as the source of the problem. The production line had a well-designed ESD program known to be in compliance with current best practices. Furthermore, a careful analysis of the line produced no indication of the reason this particular part was failing at higher than normal levels.

Other possible changes were also investigated. For example, the supplier of the IC was consulted to determine whether any changes had been made to the design that might affect its ESD withstand voltages. No such changes had been made. In fact, the device had been tested for its vulnerability to ESD and met all requirements. Most significantly, its CDM withstand voltage was 1500 V, which is well above requirements.

While investigating changes in the design or materials, it was discovered that the source of the faceplate plastic had changed around the time that the failure levels began to increase. Both the base resin and the molder had changed; it was then found that the electrostatic voltages on the faceplates were extremely high, with 10 kV being typical, and that these voltages persisted for days or weeks. Laboratory investigations then showed that the faceplates from the new source tended to charge to levels about five times higher than the previous ones, and that the charge retention was much longer.

For reasons that will become clear in this discussion, the board- and device-level FMA was difficult. Eventually, it was demonstrated that the exact failure observed in the factory could be produced by tribocharging the faceplate and then touching (grounding) the circuit pack in a particular way. This was a classic example of a field-induced CDM failure.

A sound ESD program requires a combination of good design and sound manufacturing practices.

Initial investigations into the failure mechanism of the circuit packs indicated that the pin (21 or 22) that failed in the factory (Figure 1) was not physically touched during testing or handling of the circuit pack. This was surprising because the CDM failure of a pin requires that the pin be grounded. Further laboratory studies were conducted, which confirmed that the pin 21–22 leakage current could be produced by touching a pin on a transformer mounted near the faceplate.

This pin was connected by a low-resistance bus on the PWB to pin 36 of the CMOS device (see Figure 1). Therefore, the pin that exhibited the failure was different than the pin stressed. This is not unusual for CDM events. However, this is seldom observed in routine qualification of devices, because stress testing of the device is usually done only after all pins have been stressed.

Therefore, it is important in FMA investigations to stress the device in a manner that resembles as closely as possible the actual sequence of events in order to confirm the failure mechanism.

The next step was to understand how the charging and discharging events were occurring in the factory. Subsequent investigations showed that the faceplates charged very easily during shipping and handling and were very difficult to neutralize reliably. Several scenarios for improved shipping and handling procedures were investigated. Ultimately, a materials solution emerged as the most attractive alternative. The discharges were found to be occurring during the testing of the circuit pack. The entire scenario is represented schematically in Figure 1.

When the circuit pack with its charged faceplate was placed in the bed-of-nails tester, the first test probe to touch the pack touched a pin on the transformer near the charged faceplate. The transformer pin was about a half-inch from the charged faceplate. Because the voltages on the faceplates were very high, it was easy to imagine that the effective induced voltage as seen by the transformer and device exceeded the 1500-V withstand voltage.

In conclusion, the cost of repair and replacement for this

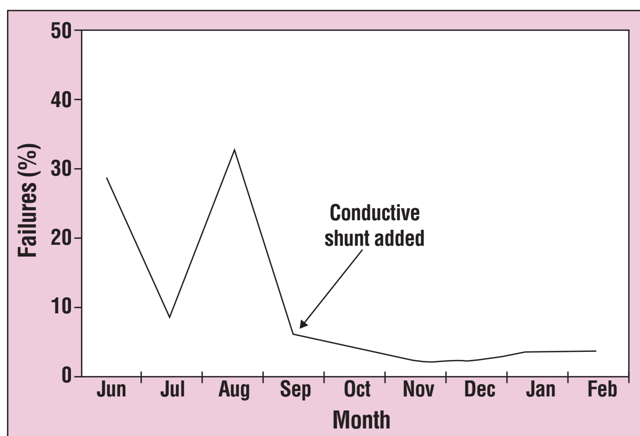

Figure 2. Circuit pack yield variation (production yield losses).

failure was estimated at between $500,000 and $1 million, not including the costs of the FMA investigations. However, the economic impact could have been much worse if the company had not had a long-standing requirement for minimum CDM performance. For example, if the CDM withstand voltage had been a 150 V, then faceplate voltages of as little as 1 kV could have produced comparable failure levels. This is significant because the solution to this problem—finding a lower-charging material—would not have been effective. Furthermore, with the high-charging material, the dropout rate could have been in the 50% range, with a cost impact of $10 million to $20 million, and the viability of the product line would have been threatened.

Case Study 2: Ultrasensitive-Device Failures on Circuit Boards. The high failure rates cited below occurred to circuit boards, dispelling Myth 2. Furthermore, special procedures had to be developed to successfully handle an ultrasensitive (Class 0) device and, thus, more than one area classification became necessary (see Myth 3).

The trend toward including ultrasensitive devices in the manufacturing process calls for a separate discussion of the problems and difficulties that can arise in handling these devices. One such case was revealed with the introduction of an N-type metal-oxide semiconductor (NMOS) device that had an ESD withstand voltage of 20 V. Major problems were encountered during device fabrication, as well as during the manufacture of PWB assemblies.

This low threshold was the result of a lack of protection circuitry on the high-speed pins of the device. The designers presumed that any such circuitry would prevent the device from performing its intended function.

PWB Assembly. Extreme fluctuations in PWB assembly yields (see Figure 2) were occurring during the start of ramp-up, the period during which production quantity begins to increase rapidly in order to meet the ultimate levels of production. Between the months of June and September, the removal rate varied dramatically between 10 and 30%. In actual lot-to-lot observation, some lots showed a 100% drop-out in which every single device was defective.

Because of the scarcity of these 20-V NMOS03 devices, the cost implications of their continued failure were very high. Therefore, a detailed investigation was undertaken. Through failure analysis, it was determined that the devices were failing due to ESD. In fact, it was demonstrated through FMA atBell Laboratories that virtually all of the failures were ESD induced. However, no solution for handling a device that failed at 20 V was readily apparent.

A special detailed audit was conducted. A number of people experienced in different aspects of the issue were consulted. A detailed inspection of the manufacturing line began, and a plan of corrective action was compiled. Based on that action plan, a task force was assembled and assigned to correct deficiencies in the line and to report weekly on what corrective measures had been taken. Because of the extreme seriousness of this situation, the weekly reports were channeled to high-level executives in the company.

Initially, many extraordinary handling precautions were instituted. Even with all of this special attention and compliance with the procedures defined by Class I sensitivities, yields continued to fluctuate dramatically from June through September (see Figure 2).

The solution to this particular problem was found in the introduction of a top hat. A top hat is a conductive shunt placed on top of a device after it has been assembled to the PWB. As soon as these problem-causing ultrasensitive devices were mounted on the PWB assembly, the shunt that electrically shorted the leads together was placed on top. The board was then allowed to go through the production line in normal sequence.

Common ESD Myths

1. "Small" companies cannot afford large-company ESD programs.
2. Printed wiring board (PWB) assemblies are not ESD sensitive.
3. One ESD sensitivity classification is sufficient for all areas.
4. Human body model (HBM) data are sufficient for detecting device sensitivity levels.
5. Airflow causes charging.
6. Metallized or highly conductive shielding layers are essential.
7. Highly conductive materials provide increased protection.
8. Grounded metal is a safe surface for ESD-sensitive components or assemblies.
9. Designed-in ESD protection precludes the need for ESD handling controls.
10. Smocks are an essential element of an ESD program.
11. The "three-foot rule" is an important ESD safeguard.
12. Touch-ground procedures are effective.
13. A one-heel grounder is sufficient protection.
14. Individuals wearing wrist straps at ESD workstations cannot damage sensitive devices or assemblies.
15. Supplier data sheets on ESD materials can be accepted without question.

The results of the inauguration of that procedure during the month of September are clearly and dramatically recorded in Figure 2. By mid-November, the removal rate had dropped even further, to around 2%. By the simple addition of a shunt to the devices, a dropout rate of 30% was reduced to 2%.

The simplicity of this solution is particularly striking in contrast to more-common procedures involving every kind of ESD-protective device known to science. The use of so many kinds of precautions eventually becomes difficult to manage. In cases such as this, when an ultrasensitive device is so easily damaged, the extraordinary measure of using a multitude of standard precautions may prove futile, as well as expensive. The solution described here introduces a simple shunt into a Class I set of procedures. The incremental cost is trivial. A total expenditure of $1000 provided the level of protection required. Yet the dollar savings realized on the production line (excluding overhead expenses) reached $6.2 million per year for this one device on this one line. That is an impressive payback by any measure.

One additional benefit derived from this case was the impact that it had on the design community. Asked to justify a withstand voltage of 20 V for the NMOS device involved in the project, designers responded by redesigning the device and raising the level of sensitivity to 1000 V HBM, a remarkable accomplishment. Some system-level design changes were made to accommodate the new protection circuitry and maintain the system performance.

This case study makes it clear that ultrasensitive devices can present a potential threat to production lines that could result in lost production and lost sales. The financial implications are particularly unattractive when the cost of lost sales is added to the cost of lost materials. In its final configuration, the PWB assembly is enclosed in a metal housing. Consequently, this ultrasensitive device has always been well protected in the field and has a low return level for ESD defects.

As a direct result of the experience outlined in this case study, minimum design requirements were modified, and a new set of handling requirements (Class 0) was established and added to requirements. It was apparent that a cookbook approach to establishing handling criteria for ultrasensitive devices would not work. For example, it is likely that some of the automated equipment used in the assembly process was causing the problem solved by the application of the top hats. Clearly, standard handling procedures specified in many industry standards did not solve this problem. An extraordinary solution tailored to the situation was required, and it was highly cost-effective.

Adding a shunt was not only necessary but sufficient to protect the device at great economic benefit. In addition, a Class I shop was allowed through this solution to continue to do business as usual while protecting an ultrasensitive device. Training considerations were minimized, and the impact on personnel significantly simplified.

Case Study 3: Latency. Although not a common myth, latency is a reliability issue. This case history was selected to illustrate latent failures due to prior ESD damage in a hybrid integrated circuit (HIC) design incorporating a bipolar silicon IC. In this example, evidence is presented of latent failures occurring during normal processing.

Experimental Evidence. The first evidence of a problem appeared in the early stages of initial production during a quality-assurance sampling when 3 out of 15 PWB assemblies failed the system test. These PWB assemblies had just passed an identical system test as part of the manufacturing process, which did not include ESD protection. Subsequent defect analysis revealed a bipolar junction on HIC "B," with excessive leakage in all three PWB assemblies. Also, the failing external HIC pin was routed directly to another HIC on the PWB, rather than to an external PWB assembly connector pin.

Later, an unrelated laboratory evaluation of 24 of the same type of PWB assemblies was initiated. The PWB assemblies were put into an operating system, tested successfully, and then left functioning in a secured area. During the next five days, 5 of the 24 PWB assemblies failed with the leakage condition described above. Figure 3 is a scanning electronic microscope (SEM) photograph (at 4800×) of the junction damage exhibited by all five failures.

Although it is difficult to see, there is a faint trace between the two conductors, indicated by the arrow. The damage was subsequently duplicated by exposure to ESD. The threshold of damage was established at 450 V HBM for HIC "B" and at 1000 V HBM for the completed PWB assembly.

The circumstances surrounding these five failures were such that no one could have touched them once they were operating in the system. Additionally, the testing was done by remote access. Therefore, it is likely that these failures were latent due to prior ESD damage.

At approximately the same time, one customer reported that 17 PWB assemblies out of 31 failed two weeks after being successfully put into service. All exhibited the same leakage condition as the five laboratory failures and were suspected of having latent ESD failures.

In comparing this failure activity to the in-house data above, a statistically significant difference is noted with a confidence level of 99%. Likewise, a review of the field data indicated that this situation was extremely abnormal. Therefore, unique and severe conditions triggered the 17 failures. Further evaluation revealed that these PWB assemblies had been expedited through unusual channels in the dry winter months and that they had been transported in expanded polystyrene (EPS) trays.

Furthermore, these PWB assemblies were child boards and required assembly to the parent board on customer premises. During assembly, it is particularly convenient and almost necessary for the installer to directly contact the conductor on the PWB leading to the indicated HIC pin, thereby increasing the probability of ESD damage. Therefore, the EPS packaging (in conjunction with the circumstances in the field) was most likely a major factor leading to latent failure. However, prior damage in the factory or in transit could not be ruled out.

Compared with the number of failures during early production, these failures were insignificant and were the only ones reported. However, on the premise that it was an early warning, response was prompt—ESD precautions were incorporated throughout the manufacturing and shipping process, and a Zener diode was added to the PWB assembly to

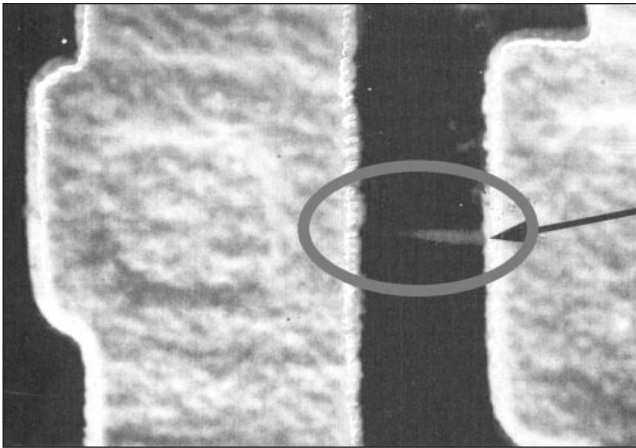

Figure 3. Latent ESD failure.

shunt ESD transients to ground. Adding the diode improved the PWB assembly threshold from 1000 V to something in excess of 15,000 V. As a longer-term solution, HIC "B" was redesigned to incorporate additional protection.

Latent failure due to prior ESD damage was witnessed under laboratory conditions. As a result of EPS packaging, ESD damage was suspected of having occurred on customer premises while the PWB assemblies were in service. This, in conjunction with other reports of latency, supports previous conclusions that ESD damage can adversely affect the reliability of bipolar devices.[3]

References

1. T Dangelmayer, *ESD Program Management*, 2nd Ed., (Boston: Kluwer Academic Publishers, 2001).
2. M Kelly et al. "A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices," in *EOS/ESD Symposium Proceedings* (Phoenix, AZ: ESD Association, 1995), 175–185.
3. OJ McAteer and RE Twist, "Latent ESD Failures," in *EOS/ESD Symposium Proceedings* (Orlando, FL: ESD Association, 1982), 41.

Bibliography

Anand, Y and Crowe, D. "Latent ESD Failures in Schottky Barrier Diodes," in *Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium Proceedings* (1999).

Bossard, PR, Chemelli, RG, and Unger, BA. "ESD Damage from Triboelectrically Charged IC Pins," in *EOS/ESD Symposium Proceedings* (1980).

Cook, C and Daniel, S. "Characterization and Failure Analysis of Advanced CMOS Sub-Micron ESD Protection Structures," in *EOS/ESD Symposium Proceedings* (1992).

Greason, WD and Chum, K. "The Integrity of Gate Oxide Related to Latent Failures Under EOS/ESD Conditions," in *EOS/ESD Symposium Proceedings* (1992).

Kim, SU. "ESD Induced Gate Oxide Damage During Wafer Fabrication Process," in *EOS/ESD Symposium Proceedings* (1992).

Renninger, RG . "Mechanisms of Charged-Device Electrostatic Discharges," in *EOS/ESD Symposium Proceedings* (1991).

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