Class 0 ESD: A Driver for Change in Assembly ESD Control Programs

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The proliferation of electronic devices with very high sensitivity to ESD necessitates a transformation of production ESD control programs.

Electrostatic discharge (ESD) controls for electronics manufacturing have been employed for decades. While there have been improvements in materials and methods of ESD control over this period, and although some factories have done a better job than others of implementing controls, the fundamental capability of the methods has not changed appreciably. As a result, there have always been vaguely defined lower-limit device thresholds where even good ESD programs have encountered great difficulty in handling and protecting a particular device during assembly.

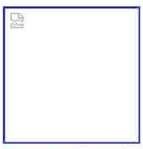

Figure 1. Evolution of the maximum allowable E-field according to the 2003 International Technology Roadmap for Semiconductors (click to enlarge).

A world-class program at AT&T, for example, was brought to a virtual standstill in 1988 by a 20-V charged-device-model (CDM) device. This happened, not because the device could not be designed with built-in protection, but, rather, because its designers determined that it would not be possible to achieve the desired performance and therefore eliminated the available protection schemes. The device was intended to operate at 1.7 GHz, which was a pioneering achievement for telephone transmission systems of the time. The specter of dealing with Class 0 devices—those with thresholds less than 200 V—in standard manufacturing environments then simmered under the surface for the decade that followed.[1]

At that time, the metal oxide semiconductor (MOS) processes involved feature sizes of about 1 µm. Further, high-speed applications such as the advanced light-wave system were rare in high-volume production. Radio-frequency (RF) and other applications were handled via specialized, usually manual, operations. But very different technological circumstances are prevalent today, and these are driving the concern about ESD and electronic devices to higher levels.

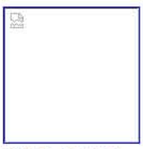

Figure 2. Downward drift of ESD threshold distribution for main populations of CMOS devices (click to enlarge).

Challenges of Evolving Technology

Today, the 90-nm technology node is in place, and 65 nm is not far off. The number of end applications poised to take full advantage of new performance capabilities increases manyfold with each succeeding generation of technology.

The 2003 edition of the Sematech International Technology Roadmap for Semiconductors includes estimates of the maximum electrostatic fields (converted to voltage units) that will be tolerated in device assembly, so-called back-end manufacturing, in the projected future (see Figure 1).[2] These estimates are based on expectations for the evolution of complementary MOS (CMOS) technology over the next decade and suggest the anticipated behavior of the major device populations as future devices are realized in the new technologies. What is expected is a general drift downward in ESD thresholds for both human-body-model (HBM) and CDM, which is represented conceptually in Figure 2.

The vast majority of future devices are expected to exhibit a robustness relative to ESD similar to that displayed by current designs as a result of the continued evolution of protection strategies through each new device generation, or technology node. However, the number of devices with low ESD thresholds can be expected to increase as well, as the lower tail of the distribution moves downward. This is the technology-node contribution to the increase in the number of Class 0
devices in production and assembly.

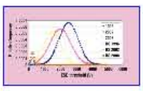

Figure 3. Bimodal ESD threshold distribution including high-speed (HS) applications (click to enlarge).

The technology node is the better known but less significant of the two main factors contributing to changes in ESD thresholds. The other main transition taking place in the electronics industry is the movement of very high speed and performance into large consumer markets. The integration of wireless telephone, camera, personal digital assistant, and computer elements in single devices is dramatically increasing the number of devices that will be performance limited in their ESD capability. Thus, the evolving threshold distribution is becoming significantly bimodal (see Figure 3).

Few low-threshold devices could be found in high-volume manufacture in 1996. RF devices typically were handled by specialty manufacturers, each of whom struggled to implement controls more stringent than was common among large manufacturers. But the combination of technology node– and performance-related forces is now creating a situation in which such devices are being introduced widely into the electronics manufacturing supply chain. The number of manufacturers that will therefore need to implement vastly improved ESD programs is increasing dramatically.

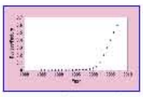

Figure 4. The number of factories handling Class 0 devices will continue to increase dramatically as more and more such devices are developed (click to enlarge).

Class 0 devices still constitute a relatively small percentage of the total device population, but it takes only one or two such devices manufactured on a continuous basis to return the risk level for a factory to that of the 1988 AT&T example (see Figure 4).

Thus, technology trends, product-level technology integration, and customer demand for wireless and high-speed products will be pushing the number of Class 0 devices upward in the near future. Most electronics assembly businesses will, as a result, have to upgrade their programs to meet this mounting challenge. The general approach to doing this is discussed next.

Class 0 Countermeasures

The implementation of Class 0 countermeasures properly begins with the acquisition of a full understanding of the ESD technology and manufacturing techniques available to offset the extreme sensitivities of this class of devices. In addition, it is necessary to realize that it is no longer business as usual, that the control techniques of Class 0 involve a paradigm shift.

Even a 50-V residual potential can cause damage to ultrasensitive components. Additional controls thus become essential. Furthermore, industry standards do not cover sensitivities less than 100 V.

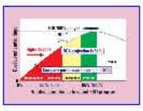

Figure 5. Return-on-assets (ROA) and return-on-investment (ROI) projections are the basis for cost-benefit analysis of a company's ESD program as compared with a fully sound program (click to enlarge).

Class 0 controls begin with flawless execution of the current best practices, such as the ESD Association standard ESD S20.20.[3] They require a total system approach that extends from product design to customer acceptance. System performance can be measured and a cost-benefit analysis graphed, as in Figure 5. This approach to representing the health of an ESD program is based on the combined impact of sound product design and manufacturing practices.[4] When the program is implemented correctly, a corresponding return on investment (ROI) develops, typically in excess of 100%.

Figure 5 also illustrates the significant ESD program improvement possible through better utilization of current assets. The return-on-assets (ROA) projection of 61% represents a 100%-plus improvement over an imaginary company's performance starting point of 30% of complete program soundness. It nearly carries the company into the range of acceptable performance. Such betterment can typically be achieved without any increase in staff head count or capital expenditures.

The special nature of Class 0 devices necessitates modifying the interpretation of the assessment, as shown in Figure 6. The main message of the plot in that figure is that, when Class 0 devices are introduced, even the ROA improvement is not sufficient to move the rating out of the zone of unacceptability.

Programs operating in the high-risk zone (as indicated in Figures 5 and 6) can pose a serious risk of catastrophic production stoppage, severe reliability failures, and lost sales revenue. Major quality and reliability busts have been known to cost companies up to $10 million per event and jeopardize millions of dollars in sales.

Figure 6. Effect of Class 0 protection on ROA and ROI in the analysis of a company's ESD program performance. Class 0 devices require a modified interpretation (click to enlarge).

Maintenance of a lower surface-resistance limit of 1 ¥ 104 ž as measured by ANSI EOS/ESD S11.11 is recommended.[5] However, the introduction of automated production equipment makes this concept difficult to implement and to measure. In the hands of a knowledgeable ESD practitioner, an electromagnetic-interference/ESD event detector can be a powerful diagnostic tool for locating sources of metal-to-metal contact.[6] The challenge is to be able to differentiate between discharge events that are damaging to product and extraneous events that, for instance, may be caused by a relay.

Conclusion

Technology, manufacturing, and product design trends are combining to drive ultrasensitive devices into mainstream production. ESD-protective techniques for handling these more-sensitive devices are not well known within the industry. However, when implemented correctly, they are not expensive or difficult to manage. In addition, industry standards cover sensitivities down to 100 V and no further. But with sound technical advice, and by taking an overall program management approach, existing ESD programs can be improved or reinvented so as to meet the challenge. Manufacturers seeking advice should be sure to get it from sources that have firsthand manufacturing and design experience with products having Class 0 sensitivities.

References

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