32ND ANNUAL EOS/ESD SYMPOSIUM & EXHIBITS

The International Technical Forum on Electrical Overstress and Electrostatic Discharge

October 3-8, 2010

John Ascuaga's Nugget Resort

Sparks, NV, USA

Register online at
esda.org/onlineregistrations.html

ONLINE REGISTRATION

IEEE

ESD ASSOCIATION®

Sponsored by the ESD Association in cooperation with the IEEE.
Technically co-sponsored by the Electron Devices Society.

General Chair's Welcome

Dear Colleagues, Friends, Supporters and Fans of the electrostatics world of research and industrial applications,

WELCOME TO YOUR 2010 EOS/ESD SYMPOSIUM!

On behalf of the ESD Association and the 2010 Symposium Steering Committee, I personally hope to greet you at the 32nd International EOS/ESD Symposium!

I am convinced that the combination of our incredible Symposium schedule of events and venue location, in the "biggest little city in the world"-Reno, Nevada, USA, will certainly give you plenty of opportunities for professional and personal development, inspiration and quality time for you and your companions!

Let me give you a quick overview on what we have planned to 'grab' your attention and time during the exciting Symposium week:

Education … It is the backbone of any activity in today's fast moving world. We start with a set of academic and professional certification Tutorials on Sunday and Monday, then continue on Thursday. Out of the 33 total tutorials, there are 4 new titles. All tutorial content was renewed by our distinguished instructors to reflect the latest research and application developments in the past year. Sign up today for the training you need!

Science… Our approach to understanding the Universe. We will begin our journey with an exciting keynote talk during the Symposium Opening and Awards Breakfast on Tuesday morning. Professor Nilton Renno of the University of Michigan, from the team who discovered water on Mars, will talk about ESD on Mars and the Moon. The Technical Program will span Tuesday to Thursday with 61 outstanding talks spread in 14 technical sessions, presenting on many hot topics related to the phenomena of static electricity and applications. Papers will be presented about semiconductor technology, products through systems robustness and manufacturing control, even issues on the space station. Please make your personal schedule and plan to meet authors and colleagues and discuss with them all the new ideas you will hear about!

Workshops… Place to share professional issues and experiences, find solutions or openly discuss ideas with supporters or critics. The program of 9 workshops on Tuesday and Wednesday afternoon will provide you the forums to talk and comment, receive feedback and learn from colleagues in a 'no necktie' environment. Prepare your hot questions today and submit them to the moderators or just start talking during your workshop!

Industry Exhibits… Generating new research challenges and offering new ESD products and services, our colleagues from many companies will be happy to meet you in the Exhibit Hall, starting with the Welcome Reception on Monday evening till the exhibits close on Wednesday afternoon. Do use this unique opportunity to find the ESD product or service you have been looking for during the year or just talk to the professionals with hands-on experience on static control methods, evaluation techniques, ESD hardware and many other ESD business matters. Complimentary coffee will be available in the exhibit hall to help these informal business and professional meetings.

Awards… Wonder whose author's team has won the 2009 Symposium Outstanding Paper Award (voted by the Symposium attendees), or the Best Paper and Best Student Paper Awards (voted by the Technical Program Committee)? Start placing bets! We are in Reno and this is quite acceptable (at least for some)! During the Symposium Awards Breakfast on Tuesday Morning, plan to hear the words "And the winner is …" for the above awards, and also for the Friendship Award, given to the authors of the Best Paper at the RCJ's ESD Symposium in Japan.

What is a Conference without good discussions and plenty of interactions? Ancient Greeks defined for the World the meaning of 'Symposium'. For them Symposium was a 'convivial meeting for drinking, music, and intellectual discussion among the participants', usually held on the shores of the warm Mediterranean sea (www.answers.com). Things since have evolved and thousands of years later I welcome you to the 2010 EOS/ESD Symposium, which, with its broad program of tutorials, workshops, and technical sessions will provide you with the unique forum to learn, share, develop and entertain and will definitively become a milestone in your professional experience!

I am looking forward to meeting you and your family at this year's event!

Dr. Vesselin Vassilev
Symposium General Chairman

Contents

ESD Association
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General Information

Register online at esda.org/onlineregistrations.html

ONLINE REGISTRATION

Information Booth

An information booth will be located in the Rose A Foyer of the *John Ascuaga's Nugget Resort* to assist you with directions, events, and general Symposium questions.

Symposium Proceedings

Each paid registrant receives one copy of the Proceedings on a flash drive. The flash drives are equipped with note taking features that allow you to save notes specific to each paper you are viewing. Printed copies of the Proceedings and additional flash drive copies are available to purchase for $150 each. Printed copies must be ordered and paid for by Aug 9, 2010, in order to receive the Proceedings on site. Use the registration form on page 31 to order.

Hospitality Suites

To maintain the objectives of the Symposium, the ESD Association encourages all exhibitors and guest organizations to schedule their hospitality and other social events at times that do not conflict with the Symposium presentations and educational activities. Adherence to this policy is appreciated.

Age Limits

No one under 18 years of age will be admitted to the Exhibit Hall.

Unauthorized Solicitation

Solicitation of business on the premises during the EOS/ESD Symposium by manufacturers or others who are not participating as exhibitors is prohibited.

Recording

Video and/or audio recording of Symposium events is prohibited without the prior written authorization of the ESD Association.

On-Site Registration Hours

Registration will be open in the Rose A Foyer at the following times:

Sunday, October 3	7:30 a.m. - 5:00 p.m.
Monday, October 4	7:30 a.m. - 5:00 p.m.
Tuesday, October 5	7:30 a.m. - 5:00 p.m.
Wednesday, October 6	7:30 a.m. - 12:00 p.m.
	2:00 p.m. - 5:00 p.m.
Thursday, October 7	7:30 a.m. - 5:00 p.m.

Registration and Fees

Save by registering in advance! This will facilitate your registration upon your arrival at the Symposium. Early registration fees are valid only if received no later than Aug 9, 2010.

	Early Registration Fees Until **Aug 9, 2010**	Registration Fees After **Aug 9, 2010**
Symposium		
ESD Association Members	$545	$745
Non-Members	$645	$745
Tutorials - ESD Association Member Prices		
Sunday (Full Day)	$495	$695
Sunday (Half Day, AM or PM)	$295	$495
Monday (Full Day)	$495	$695
Thursday (Full Day)	$495	$695
Thursday (Half Day, AM or PM)	$295	$495
Tutorials - Non-Member Prices		
Sunday (Full Day)	$595	$695
Sunday (Half Day, AM or PM)	$395	$495
Monday (Full Day)	$595	$695
Thursday (Full Day)	$595	$695
Thursday (Half Day, AM or PM)	$395	$495
Total Symposium Experience: Save with Bundled Fees		
(Symposium plus Sun., Mon. and Thurs., full tutorial days)		
ESD Association Members	$1,730	$2,410
Non-Members	$2,070	$2,410

Bundled Fees do not include S20.20 Seminar

Student Fees

The EOS/ESD Symposium offers a fifty percent discount for full-time students. Proof of enrollment is required. Student fees apply to Symposium and Tutorial registration only and do not apply to Bundled Fees or Seminar fees.

ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) (Limited to first 30 registrants)

ESD Association Members	$1,495	$1,695
Non-Members	$1,595	$1,695

This Seminar is not included in the Bundled Fees

Schedule

SUNDAY, OCTOBER 3

Registration	7:30 a.m. - 5:00 p.m.	
S20.20 Seminar (Day 1)	8:00 a.m. - 5:00 p.m.	20.20: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) (PrM)
Tutorials	8:30 a.m. - 4:30 p.m.	A: ESD Basics for the Program Manager (PrM)
	8:30 a.m. - 4:30 p.m.	B: ESD On-Chip Protection in Advanced Technologies (DD)
	8:30 a.m. - 4:30 p.m.	C: ESD Protection and I/O Design
	8:30 a.m. - 12:00 p.m.	D: System Level ESD/EMI: Principles, Design Troubleshooting, and Demonstrations
	8:30 a.m. - 12:00 p.m.	E: Triboelectrification - Theory and Applications
	8:30 a.m. - 10:00 a.m.	F: Perfect ESD Storm
	10:30 a.m. - 12:00 p.m.	G: Circuit Modeling and Simulation for On-Chip Protection (DD)
	1:00 p.m. - 4:30 p.m.	H: System Level ESD/EMI: Testing to IEC and Other Standards (PrM) (DD)
	1:00 p.m. - 4:30 p.m.	I: Use of the Digital Sampling Oscilloscope for ESD Measurements
	1:00 p.m. - 4:30 p.m.	J: ESD Ignition & Fires

MONDAY, OCTOBER 4

Registration	7:30 a.m. - 5:00 p.m.	
S20.20 Seminar (Day 2)	8:00 a.m. - 5:00 p.m.	20.20: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) (PrM)
Tutorials	8:30 a.m. - 4:30 p.m.	K: How To's of In-Plant ESD Survey and Evaluation Measurements (PrM)
	8:30 a.m. - 12:00 p.m.	L: Ionization Issues and Answers for the Program Manager (PrM)
	8:30 a.m. - 12:00 p.m.	M: SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits (DD)
	8:30 a.m. - 12:00 p.m.	N: On-Chip ESD Protection in RF Technologies (DD)
	8:30 a.m. - 12:00 p.m.	O: Troubleshooting On-Chip ESD Failures (DD)
	8:30 a.m. - 10:00 a.m.	P: Design and Application of VF-TLP and CC-TLP Systems Targeted for CDM
	10:30 a.m. - 12:00 p.m.	Q: Advanced Topics in TLP & VF TLP Testing
	1:00 p.m. - 4:30 p.m.	R: Packaging Principles for the Program Manager (PrM)
	1:00 p.m. - 4:30 p.m.	S: Device Testing-Component Level: HBM, CDM, MM, and TLP (DD)
	1:00 p.m. - 4:30 p.m.	T: Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design (DD)
	1:00 p.m. - 2:30 p.m.	U: Charged Device Model Phenomena and Design (DD)
	1:00 p.m. - 2:30 p.m.	V: HMM Basics: Standard Practice, Testing Procedures and Round Robin Study
	3:00 p.m. - 4:30 p.m.	W: CDM ESD Circuit Simulation Methods for ESD Design and Failure Debug
	3:00 p.m. - 4:30 p.m.	X: TLP Measurements: Parametric Analyzer for ESD On-Chip Protection (DD)
Reception	5:00 p.m. - 6:00 p.m.	Professional Women's Reception
Welcome Reception	6:00 p.m. - 9:00 p.m.	Exhibits Open

TUESDAY, OCTOBER 5

Registration	7:30 a.m. - 5:00 p.m.	
Awards Breakfast	7:30 a.m. (Prompt)	
Plenary Session	8:30 a.m. - 9:00 a.m.	Electrical Activity and Dust Lifting on Earth, Mars, and Beyond
Exhibits Open	9:00 a.m. - 6:00 p.m.	
Technical Sessions	9:30 a.m. - 12:00 p.m.	1A: On-Chip Physics Numerical Simulation and Modeling, Reliability Issues
	9:30 a.m. - 12:00 p.m.	1B: EOS and System Level ESD: Design and Simulation
Technical Sessions	1:00 p.m. - 3:30 p.m.	2A: ESD Electronic Design Automation: Verification and Simulation
	1:00 p.m. - 3:30 p.m.	2B: System Level ESD: Component Level ESD Correlation
Workshops A	4:00 p.m. - 5:30 p.m.	A1: Human Metal Model Testing A2: ESD Control for Class 0 Devices A3: ESD Verification Checks Leveraging Existing Commercial EDA Tools

Schedule

TUESDAY, OCTOBER 5 continued

Workshops B	6:00 p.m. - 7:30 p.m.	B1: Sources of EOS Damage and Characterization Techniques for Determining EOS Robustness
		B2: Board-Level Solutions to System-Level ESD Design
		B3: Common ESD Audit Issues

WEDNESDAY, OCTOBER 6

Registration	7:30 a.m. - 12:00 p.m.	
	2:00 p.m. - 5:00 p.m.	
Technical Sessions	8:00 a.m. - 9:40 a.m.	3A: On-Chip Protection: Advanced CMOS - Analog, Digital and Latchup
	8:00 a.m. - 9:40 a.m.	3B: Factory and Materials: CDM Related Factory Issues
	10:15 a.m. - 11:05 a.m.	3A: On-Chip Protection: Advanced CMOS - Analog, Digital and Latchup - continued
	10:15 a.m. - 11:55 a.m.	4B: Factory and Materials: New Test Methods and Materials
	11:05 a.m. - 11:55 a.m.	4A: On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 1)
Exhibits Open	9:00 a.m. - 12:00 p.m.	
ESDA Luncheon	12:00 p.m. - 2:00 p.m.	ESDA Annual Luncheon and Meeting
Technical Sessions	2:30 p.m. - 4:10 p.m.	5A: On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 2)
	2:30 p.m. - 3:45 p.m.	5B: Factory and Materials: General Interest
Workshops C	4:30 p.m. - 6:00 p.m.	C1: Equipment Grounding Issues
		C2: Challenging Pin Applications in Analog Design
		C3: ESD Challenges Due to Package Scaling and Integration

THURSDAY, OCTOBER 7

Registration	7:30 a.m. - 5:00 p.m.	
Technical Sessions	8:00 a.m. - 9:40 p.m	6A: TLP, HBM, MM, CDM - Device Testing Testers, Methods and Correlation Issues (Part 1)
	8:00 a.m. - 9:15 p.m	6B: On-Chip ESD Failure Case Studies New Mechanisms, Phenomena and Troubleshooting
	9:15 a.m. - 9:40 p.m	7B: Sub-Class 0 Devices, MR-Heads, MEMS
	10:05 a.m. - 12:10 p.m.	7A: TLP, HBM, MM, CDM - Device Testing Testers, Methods and Correlation Issues (Part 2)
	10:05 a.m. - 12:10 p.m.	7B: Sub-Class 0 Devices, MR-Heads, MEMS - continued
Tutorials	8:30 a.m. - 12:00 p.m.	Y: Cleanroom Considerations for the Program Manager (PrM)
	8:30 a.m. - 12:00 p.m.	Z: EOS/ESD Failure Models and Mechanisms (DD)
	8:30 a.m. - 12:00 p.m.	AA: Electrostatic Calculations for the Program Manager and the ESD Engineer (PrM)
	8:30 a.m. - 12:00 p.m.	BB: Automated Handling and Processes
	1:00 p.m. - 4:30 p.m.	CC: ESD Standards Overview for the Program Manager (PrM)
	1:00 p.m. - 4:30 p.m.	DD: Device Technology and Failure Analysis Overview (PrM)
	1:00 p.m. - 4:30 p.m.	EE: ESD Control for Extremely Sensitive Class 0 Devices
	1:00 p.m. - 2:30 p.m.	FF: Sensitivity of MEMS to EOS/ESD Phenomena
	3:00 p.m. - 4:30 p.m.	GG: Latch-up Physics and Design (DD)

FRIDAY, OCTOBER 8

	8:00 a.m. - 5:00 p.m.	Device Design Certification Exam
	8:00 a.m. - 5:00 p.m.	Program Manager Certification Exam
	8:00 a.m. - 5:00 p.m.	iNARTE Certification Exam

The PrM certification designation indicates those tutorials that are part of the ESD Program Manager Certification curriculum.
The DD certification designation indicates those tutorials that are part of the Device Design Certification curriculum.
There are no required tutorials or courses prior to taking the iNARTE Certification Exam, (see http://www.narte.org/h/esd.asp)

Register Online! http://esda.org/onlineregistrations.html

Plenary Session - Tuesday 8:30 a.m. - 9:00 a.m.

Electrical Activity and Dust Lifting on Earth, Mars, and Beyond

Professor Nilton O. Renno
University of Michigan
Ann Arbor, MI

Electrical activity has been measured in terrestrial and martian dust storms. The charging mechanisms, the resulting electric fields, electrical discharges, and their effects on dust lifting and atmospheric chemistry will be discussed. Finally, evidence that electrostatics is responsible for dust transport on the Moon and asteroids will be presented.

Professor Renno received a B.S. in Civil and Environment Engineering from the University of Campinas in Brazil, and a Ph.D. in Atmospheric Sciences from the Massachusetts Institute of Technology (MIT) in 1992. He was Postdoctoral Associate at MIT and Research Fellow in Planetary Sciences at the California Institute of Technology. Prior to joining the faculty at the University of Michigan in 2002, Professor Renno was Associate Professor at the Department of Planetary Sciences at the University of Arizona.

As co-investigator of NASA's 2007 mission to Mars (Phoenix), Professor Renno discovered the first direct evidence of liquid water on another planet. This finding was named one of the top stories of 2009 by Discover Magazine, National Magazine and many other media outlets. Professor Renno is co-investigator of NASA's 2010 mission to Mars (MSL) and has served on many NASA, NSF, and NRC Committees. He was a member of the Mars Exploration Rovers Atmospheric Science, and Entrance, Descent and Landing (EDL) Advisory Boards. While at the University of Arizona, Professor Renno was Associate Director of the Arizona Space Grant Consortium, Director of the University of Arizona Student Satellite Program, and Co-Chair of the National Space Grant Student Satellite Program.

Professor Renno has been making substantial contributions to our understanding of the physical processes that controls the climate of the earth and other planets and has been developing instruments to study these processes. Together with his students and collaborators he discovered theoretical and experimental evidence that pockets of liquid saline water are common on Mars shallow subsurface. Moreover, they discovered that small-scale convective plumes and vortices play an important role on the Earth's aerosol budget, that electric fields play an important role on dust lifting, and that dust electrification leads to the formation of large quantities of oxidants on Mars. This is a significant discovery because these oxidants can make the surface of Mars inhospitable to life as we know. Recently, Renno and his collaborators discovered direct evidence that large-scale electrical discharges in Martian dust storms excite global electromagnetic waves referred to as Schumann Resonance.

At the University of Michigan (UM), Professor Renno developed a multidisciplinary capstone engineering design course (ENG 450). He has been teaching ENG 450 since January 2004. In this course, teams of students from engineering and science departments work together on the design and fabrication of spaceflight instruments. Industry experts and senior engineers mentor the student teams and give guest lectures. ENG 450 students have been recruiting top jobs for junior engineers and winning student competitions. For example, they were awarded 2nd place on the prestigious NASA RASC-AL Forum in 2005 and 2006 and 1st place in 2007. According to RASC-AL organizers "Eng 450 Students are now three-for-three in three consecutive RASC-AL Competitions - a first, I believe, in nearly twenty-five years of conducting these kinds of programs for NASA!" In 2009 an Eng 450 team won the UM-OSU Air Force Challenge.

Professor Renno is a member of the American Institute of Aeronautics and Astronautics (AIAA), the Organization Scientifique et Technique Internationale du vol a Voile (OSTIV), the American Astronomical Society (AAS), the American Geophysical Union (AGU), and the American Meteorological Society (AMS), Institute of Physics, UK (IOP), International Society for Optics and Photonics (SPIE), and the ESD Association.

Welcome Reception

A Welcome Reception for all attendees will be held on Monday, October 4th at 6:00 p.m. in the Exhibit Hall. Network with your colleagues, share your ESD work experiences with others, view the exhibits, or simply pass the time meeting new people and making new friends. The 2010 Steering Committee will greet you and answer any questions regarding the Symposium.

Awards Breakfast

The annual Awards Breakfast for all registered attendees will be held Tuesday, October 5th, at 7:30 a.m. Following breakfast, General Chair Vesselin Vassilev, will officially open the Symposium. Vice General Chair, Robert Gauthier will present the 2009 EOS/ESD Symposium Paper Awards. Technical Program Chair, Michael Khazhinsky, will cover highlights of the 2010 Technical Program.

Professional and Technical Women's Reception

The Professional and Technical Women's Reception provides a friendly environment where women in the field of ESD can network and share work experiences. This year's reception will be held on Monday, October 4th, from 5:00 p.m. to 6:00 p.m.

ESDA Annual Meeting and Luncheon

The ESD Association luncheon on Wednesday, October 6th, will feature the ESD Association Annual Meeting. Association President, Donn G. Bellmore, will present the Association's annual report, including financial status, committee status and his vision for the Association's future.

Register Online! http://esda.org/onlineregistrations.html

Certification

Advance Your Career

ESD Association Professional Certification

The ESD Association offers Professional Certification for ESD Control Program Managers and for Device Design Technical Specialists. The impact of the ANSI/ESD S20.20 ESD Control Program standard on the global industry has been extraordinary. As a result, the Association recognizes the need to offer a certification program for individuals that are involved in designing, implementing, managing and auditing ESD control programs in their facilities. The Program Manager Certification program serves that purpose. In addition, the needs of the technical community for certification of various technical specialists are apparent. ESD Device Design Certification was developed for individuals that are involved in designing, testing, characterizing and implementing improved ESD protection designs. Device Design Certification demonstrates knowledge, experience and competency in the area of ESD design and test for device protection.

Requirements for certification include attending required prerequisite tutorials and passing a final exam. All of the prerequisite courses are available in the 2010 Symposium tutorial program (course list follows). Details of the Certification Programs are also available at the ESD Association booth in the registration area.

The preferred tutorial sequence for the Program Manager Curriculum is 1-ESD Basics for the Program Manager, 2-Electrostatic Calculations for the ESD Engineer, 3-Ionization Issues and Answers for the Program Manager, 4-Packaging Principles for the Program Manager, 5-System Level ESD/EMI: Testing to IEC and Other Standards, 6-Cleanroom Considerations for the Program Manager, 7-How To's of In-Plant ESD Survey and Evaluation Measurements, 8-Device Technology and FA Overview, 9-ESD Standards Overview for the Program Manager, 10-ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar).
Tutorials 2 through 6 need not be taken in the exact order, but should be attended before 7-How To's of In-Plant ESD Survey and Evaluation Measurements.

Program Manager Certification
Seminar and Tutorials

Sunday

2020	ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) (Sunday & Monday)
A	ESD Basics for the Program Manager
H	System Level ESD/EMI: Testing to IEC and Other Standards

Monday

K	How To's of In-Plant ESD Survey and Evaluation Measurements
L	Ionization Issues and Answers for the Program Manager
R	Packaging Principles for the Program Manager

Thursday

Y	Cleanroom Considerations for the Program Manager
AA	Electrostatic Calculations for the Program Manager and the ESD Engineer
CC	ESD Standards Overview for the Program Manager
DD	Device Technology and Failure Analysis Overview

Device Design Certification
Tutorials

Sunday

B	ESD On-Chip Protection in Advanced Technologies
G	Circuit Modeling and Simulation for On-Chip Protection
H	System Level ESD/EMI: Testing to IEC and Other Standards

Monday

M	SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits
N	On-Chip ESD Protection in RF Technologies
O	Troubleshooting On-Chip ESD Failures
S	Device Testing-Component Level: HBM, CDM, MM, and TLP
T	Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design
U	Charged Device Model Phenomena and Design
X	TLP Measurements: Parametric Analyzer for ESD On-Chip Protection

Thursday

Z	EOS/ESD Failure Models and Mechanisms
GG	Latch-up Physics and Design

ESDA Certification Exams

The Certified Professional-Program Manager and the Certified Professional-Device Design exams will be held on Friday, October 8th. To take either exam, applicants must have filed a registration form with the ESD Association Headquarters complete with a $50 filing fee prior to Symposium. Applicants must also have completed all required courses and had their eligibility verified by the ESD Association. An exam fee of $60 is applicable (in addition to the filing fee). Please note: Each of the test sections include essay questions that require a good understanding of English. Up to 50% of the grade in each section may involve essay and short written answers. The exam is open book. You may bring any reference materials, including, but not limited to, books, standards, and tutorial notes. You may also bring a calculator and computer. No cell phones, internet connections or sharing of reference materials is allowed.

Offer to Certified iNARTE Engineers: The ESD Association is offering iNARTE certified ESD engineers the opportunity to take the Program Manager certification exam without taking all required courses. Simply show a current iNARTE card, pay the exam fee and take the exam. Please note that the Program Manager exam covers more areas than the iNARTE exam and may be more difficult.

iNARTE Certification Exam

The iNARTE Certification exam will be offered on Friday, October 8th. Applicants must complete an application form and submit application fee to iNARTE prior to the exam. For more information on the requirements and application forms for iNARTE Certification see http://www.narte.org/h/esd.asp.

Education

Track Designation The TFAS track designation indicates those tutorials that are part of Track 1: ESD Test, Failure Analysis, and Systems. The FMEC track designation indicates those tutorials that are part of Track 2: Factory, Materials, and ESD Control. The DDT track designation indicates those tutorials that are part of Track 3: Device, Design, and Technology.

Track 1 (TFAS)
ESD Test, Failure Analysis, and Systems

Sunday

D System Level ESD/EMI: Principles, Design Troubleshooting, and Demonstrations
H System Level ESD/EMI: Testing to IEC and Other Standards
I Use of the Digital Sampling Oscilloscope for ESD Measurements

Monday

O Troubleshooting On-Chip ESD Failures
P Design and Application of VF-TLP and CC-TLP Systems Targeted for CDM
Q Advanced Topics in TLP Testing & VF TLP Testing
S Device Testing-Component Level: HBM, CDM, MM, and TLP
V HMM Basics: Standard Practice, Testing Procedures and Round Robin Study
X TLP Measurements: Parametric Analyzer for ESD On-Chip Protection

Thursday

Z EOS/ESD Failure Models and Mechanisms
AA Electrostatic Calculations for the Program Manager and the ESD Engineer
DD Device Technology and Failure Analysis Overview

Technical Sessions

1A On-Chip Physics Numerical Simulation and Modeling, Reliability Issues
1B EOS and System Level ESD: Design and Simulation
2B System Level ESD: Component Level ESD Correlation
6A TLP,HBM,MM,CDM Device Testing Testers, Methods and Correlation Issues (Part 1)
6B On-Chip ESD Failure Case Studies New Mechanisms, Phenomena and Troubleshooting
7A TLP,HBM,MM,CDM Device Testing Testers, Methods and Correlation Issues (Part 2)

Workshops

C3 ESD Challenges Due to Package Scaling and Integration

Track 2 (FMEC)
Factory, Materials, and ESD Control

Sunday

A ESD Basics for the Program Manager
E Triboelectrification - Theory and Applications
F Perfect ESD Storm
J ESD Ignition & Fires

Monday

K How To's of In-Plant ESD Survey and Evaluation Measurements
L Ionization Issues and Answers for the Program Manager
R Packaging Principles for the Program Manager

Thursday

Y Cleanroom Considerations for the Program Manager
BB Automated Handling and Processes
CC ESD Standards Overview for the Program Manager
EE ESD Control for Extremely Sensitive Class 0 Devices

Technical Sessions

3B Factory and Materials: CDM Related Factory Issues
4B Factory and Materials: New Test Methods and Materials
5B Factory and Materials: General Interest
7B Sub-Class 0 Devices, MR-Heads, MEMS

Workshops

A3 ESD Verification Checks Leveraging Existing Commercial EDA Tools
B1 Sources of EOS Damage and Characterization Techniques for Determining EOS Robustness
B3 Common ESD Audit Issues
C1 Equipment Grounding Issues

Track 3 (DDT)
Device, Design, and Technology

Sunday

B ESD On-Chip Protection in Advanced Technologies
C ESD Protection and I/O Design
G Circuit Modeling and Simulation for On-Chip Protection
H System Level ESD/EMI: Testing to IEC and Other Standards

Monday

M SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits
N On-Chip ESD Protection in RF Technologies
O Troubleshooting On-Chip ESD Failures
T Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design
U Charged Device Model Phenomena and Design
W CDM ESD Circuit Simulation Methods for ESD Design and Failure Debug

Thursday

Z EOS/ESD Failure Models and Mechanisms
DD Device Technology and FA Overview
FF Sensitivity of MEMS to EOS/ESD Phenomena
GG Latch-up Physics and Design

Technical Sessions

1A On-Chip Physics Numerical Simulation and Modeling, Reliability Issues
2A ESD Electronic Design Automation: Verification and Simulation
3A On-Chip Protection: Advanced CMOS-Analog, Digital and Latchup
4A On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 1)
5A On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 2)
6B On-Chip ESD Failure Case Studies New Mechanisms, Phenomena and Troubleshooting
7B Sub-Class 0 Devices, MR-Heads, MEMS

Workshops

A1 Human Metal Model Testing
A2 ESD Control for Class 0 Devices
B2 Board-Level Solutions to System-Level ESD Design
C2 Challenging Pin Applications in Analog Design

Seminar

SUNDAY & MONDAY, OCTOBER 3 & 4

Seminar 20.20: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar)

8:00 a.m. - 5:00 p.m.
Certification: PrM
Ron Gibson; John T. Kinnear, IBM

Space Limit
This course is limited to a maximum of 30 attendees, on a first-come, first-serve basis.

This seminar provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The course provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certification requirement for in-plant auditors and program managers who are working toward professional ESD certification. The following topics are covered in this course:

- Overview of ANSI/ESD S20.20
- ESD program assessment
- Overview of the assessment process
- How to approach an assessment
- ESD program techniques for different applications
- The audit checklist and follow-up questions
- Administrative elements
- Technical elements

It is recommended that the ESD Program Development and Assessment Seminar be taken after the Certification candidate has taken most of the other Program Manager related tutorials.

Tutorials

Tutorials: A full, three-day program of educational tutorials provides opportunities for in-depth exploration of specific topic areas. Featuring basic, intermediate, and advanced courses, the tutorial program is organized along parallel tracks to allow attendees to easily create an individual educational experience in specific categories of interest (see box on page 6). Attendees may select courses from any track.

Certification Designation: The PrM certification designation indicates those tutorials that are part of the ESD Program Manager Certification curriculum. The DD certification designation indicates those tutorials that are part of the Device Design Certification curriculum.

SUNDAY, OCTOBER 3

Tutorial A: ESD Basics for the Program Manager

8:30 a.m. - 4:30 p.m.
Certification: PrM Track Designation: FMEC
Stephen Halperin, SH&A/Prostat Corporation
Technical Level: Basic

This presentation is a comprehensive introduction to the fundamentals of ESD causes and control. ESD Basics is a full-day seminar consisting of three presentation sections. Part 1 includes an overview of ESD impact on industry, detailed explanations of Charge Generation, Field Measurement, the role of Capacitance and Voltage, Charge Measurement and Charge Decay. Part 2 focuses on general explanations and illustrations of Device Failure Mechanisms, including Human Body Model, Charge Device and Field Induction Modes, and explains the Machine Model. Part 3 is concerned with protecting ESD sensitive devices & assemblies, defining the Electrostatic Protected Area (EPA), understanding various ESD control elements and material selection, and includes a brief introduction to ANSI/ESD S20.20 ESD Program Development criteria. Several demonstrations and opportunities for discussion make this an interesting introduction to ESD causes and control. No previous ESD experience necessary.

Tutorial B: ESD On-Chip Protection in Advanced Technologies

8:30 a.m. - 4:30 p.m.
Certification: DD Track Designation: DDT
Charvaka Duvvury, Texas Instruments, Inc.
Technical Level: Intermediate/Advanced

This tutorial addresses the important issues for the design of IC protection circuits built with advanced deep sub-micron CMOS technologies, including silicon-on-insulator (SOI) and high voltage MOSFETs for analog applications. This tutorial will present fundamental aspects of ESD protection design such as basic NMOS and SCR concepts, gate-biased and substrate-driven NMOS protection techniques, as well as some advanced low capacitance and high speed protection devices. Protection design methods to meet the human body model (HBM), machine model (MM), and charged device model (CDM) will be presented. Other topics to be covered include BiCMOS protection, circuits, mixed voltage protection and compatibility to latch-up, and an overall system on chip (SoC) protection strategy. Specific design examples will be presented to assist in understanding the methods for design synthesis. This tutorial should be useful for design, device, process, product, failure analysis, and reliability engineers and will assist those attending other design related tutorials. Attendees should have a minimum knowledge of MOS device operation in integrated circuits.

Tutorial C: ESD Protection and I/O Design

8:30 a.m. - 4:30 p.m.

Track Designation: DDT

Nathaniel Peachey, RF Micro Devices; Michael Stockinger, Freescale Semiconductor

Technical Level: Advanced

This tutorial is intended to provide the attendees with the tools to take a device level understanding of ESD protection circuits and implement them effectively in I/O designs. Beginning with a short review of ESD protection strategies, this course will focus more directly on equipping the ESD engineer to build basic I/O structures or cells along with design guidelines such that the circuit designer can implement them into an ESD robust pad ring. This tutorial will cover bus line structures, multiple power domain considerations, and an overview of the various I/O cells typically required by the circuit designer such as digital, mixed signal, RF, and analog. Finally this tutorial will touch on several of the more complex circuits that the ESD engineer may need to consider; such as noisy power rails, signals that swing below ground or above the power rail, and high voltage pins.

Tutorial D: System Level ESD/EMI: Principles, Design Troubleshooting, and Demonstrations

8:30 a.m. - 12:00 p.m.

Track Designation: TFAS

Douglas Smith, D.C. Smith Consultants

Technical Level: Intermediate

This System Level ESD tutorial will cover several facets of ESD as applied to electronic systems. Many of the principles and troubleshooting techniques will be demonstrated on real circuits for the students, with several new experiments added since previous years. "War" stories will also be used to illustrate points. The emphasis will be on making the experience both entertaining and informative for the students using an intuitive approach without heavy mathematics. Topics covered will include 1) Characteristics of ESD events; 2) ESD principles as applied to electronic systems; 3) Design troubleshooting techniques; 4) Unusual forms of ESD that have been the cause of field failures including internal chair discharges; 5) High-frequency measurement techniques; and 6) System design principles. It is recommended that those attending this tutorial section have at least one year of a college level electronics circuits course. Knowledge of common circuit analysis techniques will be assumed.

Tutorial E: Triboelectrification - Theory and Applications

8:30 a.m. - 12:00 p.m.

Track Designation: FMEC

William D. Greason, University of Western Ontario

Technical Level: Intermediate

Triboelectrification refers to the process whereby two materials become charged after contact and separation. It is one of the prime charge generation processes involved in electrostatic discharge (ESD) events. This tutorial reviews the theory of triboelectrification, its measurement and control. Work function theory is used to predict the polarity of the charge exchange during contact; the nature of the surfaces, the effective contact area and environmental conditions affect the net charge which remains after separation. Techniques for measuring the charging characteristics of materials are presented and the results of tests to study the effect of temperature and humidity are provided. Methods to limit charge levels by the control of generation and dissipation processes are discussed. A brief review of some of the beneficial applications of triboelectrification, such as electrostatic painting, xerography and material separation, is also included.

Tutorial F: Perfect ESD Storm

8:30 a.m. - 10:00 a.m.

Track Designation: FMEC

Ted Dangelmayer, Dangelmayer Associates LLC

Technical Level: Intermediate

Learn how to prepare for the "Perfect ESD Storm" that is brewing in the electronics industry. The trend towards extensive use of ultra-sensitive components (Class 0) and the widespread lack of CDM (Charged Device Model) understanding are brewing the "Perfect ESD Storm." It is no longer business as usual, and it can take up to two years to prepare. This tutorial is intended for professionals who have a basic understanding of ESD but are not fully aware of CDM control techniques or the industry trend toward extremely sensitive devices and the counter measures that are necessary. Learn the answers to your questions as well as these examples. Are you skeptical about this news of a Class 0 trend? Is it really happening? Is it likely to be a problem in your factory? How big a problem is CDM in manufacturing? What is different about CDM controls? How do I tailor ANSI/ESD S20.20 for CDM and Class 0? Join us for this highly interactive tutorial and learn why this is inevitable and how to prepare for it.

Tutorial G: Circuit Modeling and Simulation for On-Chip Protection

10:30 a.m. - 12:00 p.m.
Certification: DD Track Designation: DDT
Elyse Rosenbaum, University of Illinois at Urbana-Champaign
Technical Level: Intermediate/Advanced

This tutorial addresses modeling and simulation of protection circuit elements and networks under ESD conditions. The high-current characteristics and transient responses of devices typically used in ESD protection circuits will be presented. The objective is to ascertain what behaviors have to be captured in models intended for circuit-level simulation of ESD. Specific examples of model implementations will be provided. Parameter extraction and model scalability will be addressed. Thermal modeling will be discussed, as will be the issue of modeling the off-state behavior of ESD protection devices. This tutorial assumes some familiarity with device physics. It is directed toward persons with an interest in the transistor-level physics of ESD in on-chip protection circuits and an interest in computer-aided design.

Tutorial H: System Level ESD/EMI: Testing to IEC and Other Standards

1:00 p.m. - 4:30 p.m.
Certification: DD, PrM Track Designation: TFAS/DDT
Michael Hopkins, EM Test
Technical Level: Intermediate

This tutorial is intended to help those tasked with testing products to IEC and other System Level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences among IEC, ANSI, Telcordia and some automotive ESD standards. We will answer common questions regarding test set-ups, test points and procedures, and address key issues, including: 1) Differences between "verification" and "calibration" and when is each required; the influence of ESDA WG14. (TR) on IEC and how it affects the calibration and verification procedures. 2) Test set-up requirements, the test environment, ground connections, and return paths and ground plane effects. 3) Testing procedures with demonstration on actual products, how the tester affects test results, and problems with test result variations due to simulator influences. 4) What points need to be tested and why, guidance on determining "operator accessible" points and ports, exempted points and ports, and what to do around connectors and connector pins. 5) ANSI and other ESD Standards, the drive toward harmonization with IEC, why standards will probably never be the same as IEC, the scope of different standards. This System Level ESD tutorial will cover several facets of ESD as applied to electronic systems.

Tutorial I: Use of the Digital Sampling Oscilloscope for ESD Measurements

1:00 p.m. - 4:30 p.m. ***NEW***
Track Designation: TFAS
Larry B. Levit, LBL Scientific
Technical Level: Intermediate

The digital sampling oscilloscope (DSO) finds application in measuring waveforms that occur infrequently or only once. Its sophisticated calculation and display capabilities give it utility for factory ESD, as well as, its role in monitoring ESD immunity waveforms for both component and system level ESD.Understanding instrument performance issues is important for proper use. DSO bandwidth and the sampling rate are often used interchangeably, although they serve completely different purposes. The bandwidth, sampling rate and memory depth of the instrument must be specified for the intended application. DSOs also have display modes which can hide undersampling artifacts and lead to incorrect conclusions. Selecting the appropriate display algorithm is important for both cosmetic purposes and to achieve correct results from the instrument. Also important for the proper use of any oscilloscope are selection of the input impedance and the setup of the trigger. For a DSO, the pretrigger value must also be set. In some cases equivalent time sampling can be used but in most ESD measurements, single shot acquisition is required. Finally, for ESD applications on the factory floor, there are a variety of probes that are used. These include, wide bandwidth current probes, clamp on current probes, single ended and differential voltage probes, as well as, high frequency antennas.

Tutorial J: ESD Ignition & Fires

1:00 p.m. - 4:30 p.m.
Track Designation: FMEC
Stephen Fowler, Fowler Associates, Inc.
Technical Level: Basic

This tutorial covers the basics of electrostatic ignition, its sources, and methods for prevention. It will also cover the issues of personnel comfort around extreme charging situations such as moving webs and media. Case studies of fires, explosions, and personnel injuries will be included in the class. The class is intended to present the issues of ignitions from ESD and to have open discussions of specific needs of the attendees. The result of attending this tutorial should be a safer environment for the company and its personnel.

MONDAY, OCTOBER 4

Tutorial K: How To's of In-Plant ESD Survey and Evaluation Measurements

8:30 a.m. - 4:30 p.m.
Certification: PrM Track Designation: FMEC
Ted Dangelmayer, Dangelmayer Associates LLC; Carl Newberg, MicroStat Laboratories, Dangelmayer Associates LLC
Technical Level: Basic

Compliance verification is one of the most important elements of ESD program management and there are many technical and administrative pitfalls that can be avoided. The attendee will learn not only how to make valid auditing measurements in accordance with ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials, but also how to recognize and avoid common pitfalls. Common instruments will be explained as well as the invalid test results that can result when they are used incorrectly. Advanced auditing techniques will also be covered that enable Class 0 devices to be handled successfully. There are many ways to administer effective Compliance Verification programs. Two successful examples will be presented that were developed independently by different companies. Hidden administrative pitfalls that often result in poor compliance will also be discussed. This tutorial will be highly interactive with live demonstrations, in-plant photographs, and compelling video clips. Students will be encouraged to ask questions and to participate in the discussions.

Tutorial L: Ionization Issues and Answers for the Program Manager

8:30 a.m. - 12:00 p.m.
Certification: PrM Track Designation: FMEC
Arnold J. Steinman, Electronics Workshop
Technical Level: Basic

The primary method of static charge control is direct connection to ground for conductors, static dissipative materials, and personnel. But a complete static control program must also deal with isolated conductors, insulating materials, and moving objects that cannot be grounded. Air ionization can neutralize the charge on insulated and isolated objects. This seminar will present the information needed to use ionizers to solve problems caused by static charge. It will first examine the problems caused by static charges in a variety of workplaces, and then review the common methods by which static charges are generated and controlled. Demonstrations will be done to illustrate basic principles, leading to an understanding of why ionizers must be included in a static control program. The major types of ionizers and their use environments will be explained. Electrical and performance test methods will be discussed in detail. Ionization measurements using the Ionization Standard will be demonstrated. Installation, safety, maintenance, and contamination issues will be presented. Finally, a number of case histories will be analyzed illustrating the use of ionizers in a variety of work environments.

Tutorial M: SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits

8:30 a.m. - 12:00 p.m.
Certification: DD Track Designation: DDT
James Miller, Freescale Semiconductor, Inc.
Technical Level: Intermediate/Advanced

Over the past 15 years, there has been a gradual evolution in ESD protection for advanced technology CMOS ICs. On-chip ESD networks built with non-snapback ESD devices and circuits, including simple forward biased diodes and active MOSFET rail clamp circuits, have increasingly replaced once-prevalent networks built with snapback ESD devices, including avalanche-triggered lateral bipolar transistors and SCRs. Non-snapback devices enjoy several advantages in process portability, scalability, layout area and ease of compact modeling for circuit simulations in SPICE. In this tutorial we will explore in turn each of the key elements in active ESD networks; including typical options for diodes and active clamp devices with trigger circuits. We will cover in detail the important role that buss resistance plays in determining the optimum size and placement of clamps in a bank of I/O cells. We will also review approaches for adding secondary protection and for ESD-hardening of fragile output driver transistors. Next a step-by-step methodology for SPICE-based ESD network design and optimization will be introduced. Finally, the flexibility of active ESD networks will be demonstrated in a wide range of IC application examples.

Tutorial N: On-Chip ESD Protection in RF Technologies

8:30 a.m. - 12:00 p.m.
Certification: DD Track Designation: DDT
Steven H. Voldman, Intersil Corporation
Technical Level: Intermediate/Advanced

In this tutorial, electrostatic discharge (ESD) protection in radio frequency (RF) technologies is discussed. It covers ESD protection in RF CMOS, BiCMOS silicon germanium, gallium arsenide, and RF silicon-on-insulator (SOI). This tutorial will focus on device physics, technology, ESD layout design, ESD circuits and design systems. Also HBM, MM and TLP measurements of RF ESD technologies and RF circuits will be shown.

Tutorial O: Troubleshooting On-Chip ESD Failures

8:30 a.m. - 12:00 p.m.
Certification: DD Track Designation: TFAS, DDT
Hans Kunz, Texas Instruments, Inc.
Technical Level: Intermediate/Advanced

Diagnosing and fixing on-chip ESD product qualification failures can often be one of the more challenging aspects of work in ESD. The pressure to quickly find and correct an HBM/MM/CDM failure in order to qualify a product often compounds the inherent difficulty of troubleshooting. Experience diagnosing failures, though not desirable from a product qualification standpoint, can greatly improve troubleshooting skills. This tutorial will build troubleshooting experience and skills by presenting case studies of actual on-chip HBM failures in a workshop format. The evidence for each case will be revealed and the failure analyzed in the same manner as an actual failure. Participants will be led through and allowed to analyze each failure case, interacting with the instructor to determine its root cause and a solution. This tutorial will identify common concepts, methods, and tools useful in failure diagnosis. Participants should be familiar with CMOS technology, on-chip ESD breakdown phenomena, standard ESD protection circuits, and the HBM test procedure. Participants should also be acquainted with basic CMOS circuit design, should be able to read circuit diagrams, and should have a basic understanding of the function of IO circuits.

Tutorial P: Design and Application of VF-TLP and CC-TLP Systems Targeted for CDM

8:30 a.m. - 10:00 a.m.
Track Designation: TFAS
Horst A. Gieser, Fraunhofer IZM
Technical Level: Intermediate

Transmission Line Pulse (TLP) systems are key tools for successful development of ESD protection. Since 1985, industry and academia have built a variety of TLP-system configurations where their source impedance and method of pulse metrology are different. Most of them employ 100 ns square pulses that rise within less than 10 ns, similar to the HBM pulse parameters. “Very Fast” TLP systems with 3 ns pulse lengths address the CDM time scale events, characterize the initial turn on of the protection circuits, but analyze the high current behavior with less self heating than 100 ns pulses, and they show oxide breakdown. This tutorial not only explains the construction principles of the different TLP systems, but also provides useful hints for building, operating and calibrating a system.

Tutorial Q: Advanced Topics in TLP & VF-TLP Testing

10:30 a.m. - 12:00 p.m.
Track Designation: TFAS
Evan Grund, Grund Technical Solutions, LLC
Technical Level: Intermediate

Seminars in TLP have been focused on introductions to TLP or specific topics, such as VF-TLP. Some TLP theory is needed to move from the basic TLP use to making good measurements on a wide variety of devices under test. The first goal is to provide this theoretical understanding behind the TLP measurement. Many configurations of TLP are in use today as described in the ANSI/ESD SP5.5.1. The second goal is to understand TLP configuration differences and trade-offs. The last goal is to learn how to improve accuracy of measurements with better TLP calibrations, and to interpret data from differently calibrated TLP systems. Several additional topics of general interest will be included as time permits.

Tutorial R: Packaging Principles for the Program Manager

1:00 p.m. - 4:30 p.m.
Certification: PrM Track Designation: FMEC
David E. Swenson, Affinity Static Control Consulting, LLC
Technical Level: Basic/Intermediate

Shipping electronic parts within a factory, to another factory, distributor, or to an end-user has always been an area of uncertainty within the manufacturing process. To provide clear-cut information on what type of controlled packaging should be used in any situation, the ESD Association released a comprehensive revision of the obsolete industry standard EIA 541-1988. The newer document, ANSI/ESD S541, is the focus of this inclusive session. It provides information and guidance, as well as material specifications, to assist in the design and implementation of a packaging plan for use within an ANSI/ESD S20.20 based ESD Control Program. Current and newly released test method standards suitable for packaging material evaluation will be described. Course credit applies to the ESD Program Manager Certification curriculum. Previous attendance at the "ESD Basics" and "How To's…" tutorials are highly recommended.

Tutorial S: Device Testing-Component Level: HBM, CDM, MM, and TLP

1:00 p.m. - 4:30 p.m.
Certification: DD Track Designation: TFAS
Leo G. Henry, ESD/TLP Consultants, LLC
Technical Level: Basic/Intermediate

This tutorial addresses the basics of HBM, CDM, MM, and TLP ESD stress testing of the ESD protection structures of ICs. The differences among these models will be emphasized, and then used to show how the different circuit parasitics affect the waveforms from each model-type simulator. The importance of doing ESD testing as an integral part of a high-quality component development, and qualification efforts will be stressed. Since industry-wide TLP testing is fairly new, the tutorial will cover constant impedance and constant current TLP testing, and also the TLP I-V-L characteristic plots including the snapback trigger voltages (Vt1) and currents (It1). The evolution of the leakage current (L) as it relates to the failure (It2) point will be emphasized, as well as the comparisons and correlations between HBM and TLP testing. Standards issues and test procedures will be discussed, and some comparisons will be made between the ESDA and JEDEC ESD standards.

Tutorial T: Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design

1:00 p.m. - 4:30 p.m.
Certification: DD Track Designation: DDT
Gianluca Boselli, Texas Instruments, Inc.
Technical Level: Advanced

This advanced tutorial will extensively discuss the impact of silicon technology scaling on ESD device behavior and on subsequent optimization of ESD protection design. Both Digital (CMOS) and Analog (Analog and High-Voltage CMOS, RF CMOS/BiCMOS, SOI BiCMOS, and Smart-Power) technologies will be considered. On the Digital side, the physics of CMOS components under high current conditions will be reviewed. Technology trends for sub-100 nm nodes and their implications for the ESD design window will be covered. Sub-50 nm technology challenges will be also presented. On the Analog side, the physics of Analog components (such as Schottky diodes, Power diodes, Bipolar transistors, High-Voltage SCRs, LDMOS and DEMOS) under ESD conditions will be analyzed in detail. This class is intended for individuals who have taken the basic on-chip protection class, and are familiar with basic device physics for both ESD and latch-up.

Tutorial U: Charged Device Model Phenomena and Design

1:00 p.m. - 2:30 p.m.
Certification: DD Track Designation: DDT
Michael Chaine, Micron Technology
Technical Level: Intermediate/Advanced

This course teaches the basic ESD circuit design concepts and ideas required to design-in for Charge Device Model ESD tests. It covers a brief history of CDM ESD development, charge and discharge physics, CDM failures mechanisms, and CDM design-in strategies and characterization. This course focuses on what type of circuits fail during a CDM discharge event and teaches the different types of ESD design circuit strategies that can be applied to protect those circuits. This is an introductory class, but the student is assumed to already have a basic understanding of the CDM test method.

Tutorial V: HMM Basics: Standard Practice, Testing Procedures and Round Robin Study

1:00 p.m. - 2:30 p.m. NEW

Track Designation: TFAS

Kathleen Muhonen, Penn State University

Technical Level: Intermediate/Advanced

This tutorial is an introduction to the new standard test method Human Metal Model. This standard test method highlights how to apply the system level IEC test to individual components. The waveform and its critical specifications will be discussed. The list of qualified equipment to deliver this waveform will be examined, with a focus on ESD Guns and an introduction to 50 ohm Pulsers. Other equipment necessary to conduct the test will also be covered. Set-up details of three test configurations will be discussed. Test Fixture Board specifications will be reviewed along with waveform verification procedures. The current study done by Workgroup 5.6, Round Robin Testing for HMM, will be presented including the structures used, equipment and results. Known HMM pitfalls will be investigated along with a look at the future of HMM testing.

Tutorial W: CDM ESD Circuit Simulation Methods for ESD Design and Failure Debug

3:00 p.m. - 4:30 p.m. NEW

Track Designation:DDT

Melanie Etherton, Freescale Semiconductor, Inc.

Technical Level: Intermediate/Advanced

Charged Device Model (CDM) ESD is an increasingly important reliability issue in the semiconductor industry. To prevent damage from CDM events in integrated circuits, the capability to predict and optimize the robustness of integrated circuit for these events is essential. This tutorial provides a detailed insight into CDM circuit simulation requirements that are not in the scope of other tutorials. Physical aspects of the CDM ESD phenomenon that are important for reproducing the event with circuit simulation will be taught. This tutorial teaches modeling techniques for CDM specific device physical effects and for CDM tester, package and chip parasitics, which are all necessary for accurate circuit simulation. This course also discusses methods for simplified CDM circuit simulations where detailed information is either not available or too complex to simulate. The participant also learns about the impact of the challenges of CDM ESD testing on the design and best practices to avoid associated issues. The attendees of this class are expected to have an improved appreciation of the physical effects during CDM ESD events. This knowledge can be applied to reproduce these events with circuit simulation to predict the CDM robustness of a circuit or to debug failures and failure mechanisms caused by CDM ESD stress.

Tutorial X: TLP Measurements: Parametric Analyzer for ESD On-Chip Protection

3:00 p.m. - 4:30 p.m.

Certification: DD Track Designation: TFAS

Robert A. Ashton, OnSemiconductor

Technical Level: Intermediate

The Transmission Line Pulse (TLP) technique has often been called the Parametric Analyzer for On-Chip ESD Protection. The TLP system utilizes rectangular pulses at current levels and time scales similar to Human Body Model (HBM) events. The rectangular pulse of a TLP system allows the measurement of current-voltage (I-V) curves from which can be extracted a variety of device and circuit parameters. These parameters cannot be easily measured with the double exponential pulse characteristic of HBM. This tutorial will explore the parameters to be measured with a TLP system and discuss the importance of the parameters in the design of on-chip ESD protection circuits. Circuit elements and circuits that will be discussed include n and p MOS transistors, npn bipolar transistors, diodes, resistors, metal runners, and power supply clamps. The variations in the test structure layouts, important for understanding the properties of an integrated circuit technology, will be examined. The importance of TLP source impedance on results and the measurement of turn on properties will also be discussed.

THURSDAY, OCTOBER 7

Tutorial Y: Cleanroom Considerations for the Program Manager

8:30 a.m. - 12:00 p.m.
Certification: PrM Track Designation: FMEC
Chris Long, IBM
Technical Level: Intermediate

Cleanrooms and clean environments are enabling technologies required for the manufacture of many products that have exacting contamination control requirements in order to achieve defined yield and reliability targets. Clean manufacture is required in the semiconductor, hard disk drive, flat panel display, and pharmaceutical industries, to name a few. Requirements of cleanroom/clean environments and tooling therein result in low humidity levels, low surface contamination levels, use of process-required insulators, and a lack of natural ions in the controlled environment. These factors can contribute to development of elevated static charge levels in close proximity to sensitive product, presenting both a contamination and electrostatic discharge exposure. This tutorial will provide a detailed review of the following concepts:

- Cleanroom/clean environment function
- Airborne particle classification standards
- Cleanroom compliance monitoring test methodologies
- Electrostatic attraction relation to airborne and surface contamination
- Electrostatic discharge concerns
- Cleanroom static charge generation challenges and control methodologies

In addition, several case studies of static charge control issues in clean environments will be presented.

Tutorial Z: EOS/ESD Failure Models and Mechanisms

8:30 a.m. - 12:00 p.m.
Certification: DD Track Designation: TFAS, DDT
Steven H. Voldman, Intersil Corporation
Technical Level: Advanced

Fundamental failure mechanisms of electrical overstress/electrostatic discharge (EOS/ESD) and the physics behind them are the focus of this tutorial. Topics include the primary thermal failure mechanisms, junction burnout, oxide punch-through, and metallization burnout. Particular emphasis will be placed on the concept of simulation fidelity, which is crucial in the design of meaningful and robust ESD tests. Simulation fidelity is obtained by considering the interplay of the stress environment with the failure mechanism. Because this approach is developed for arbitrary stress environments, the considerations are equally applicable to EOS environments.

Tutorial AA: Electrostatic Calculations for the Program Manager and the ESD Engineer

8:30 a.m. - 12:00 p.m.
Certification: PrM Track Designation: TFAS
Leo G. Henry, ESD/TLP Consultants, LLC
Technical Level: Intermediate/Advanced

This tutorial focuses on the basic calculations and techniques of use to the Program Manager and the ESD engineer. The content is at the introductory college pre-calculus and introductory college physics level set in the context of electrostatic discharge and its effects. It is suggested that the student gain some familiarity with these subjects prior to the tutorial. Topics covered include the electric force, the electric field and Coulombs law, electric potential and voltage. Gauss' Law is discussed as it relates to the electric field, induction and the Faraday cup. The capacitance in Q = CV is used to explain charge sharing. RC decay is discussed as it relates to ESD discharge from humans, devices, wrist straps and materials. After completing this course, the attendee should leave with a proper understanding of the differences among the calculations for peak current, power, energy and threshold voltage for a simple device.

Tutorial BB: Automated Handling and Processes

8:30 a.m. - 12:00 p.m.
Track Designation: FMEC
Donn Bellmore, Advanced ESD Services +
Technical Level: Basic/Intermediate

Is your Automatic Handling Equipment (AHE) capable of safely processing the devices of today and future technologies with lower ESD thresholds? What is proper grounding used in AHEs and what should you look for? When ordering new equipment what should you specify? What should your acceptance criteria be? What are the proper materials and designs to establish effective ground paths through the equipment? And finally, how do you measure them? This course will focus on the grounding and material requirements of ESD Controls in AHEs for prevention of CDM and MM type damage to ESD sensitive devices. Design methods and material selections that provide effective ground paths through the assembly will be introduced. Test methods used to qualify the design will be discussed. Participants will also become familiar with different types of plating and practices to provide effective ESD Control in the designs.

Tutorial CC: ESD Standards Overview for the Program Manager

1:00 p.m. - 4:30 p.m.
Certification: PrM Track Designation: FMEC
David E. Swenson, Affinity Static Control Consulting, LLC
Technical Level: Basic/Intermediate

The ESD Association's introduction of the Program Manager Certification curriculum has created a need to modify the Standards Tutorial that has been presented for a number of years, mainly to help individuals prepare for the iNARTE Engineering and Technician Exams. Currently, many of the ESDA Standards and Standard Test Methods are discussed in depth in the individual tutorials related to the specific subject matter. This Standards Tutorial provides an overview of all the Standards, grouped into common test types, based on measurement probe and test instruments. A common methodology is used in this tutorial to cover the requirements, applications and specifications for each Standard and Standard Test Method.

Tutorial DD: Device Technology and Failure Analysis Overview

1:00 p.m. - 4:30 p.m.
Certification: PrM Track Designation: TFAS, DDT
Leo G. Henry, ESD/TLP Consultants, LLC
Technical Level: Basic/Intermediate

This tutorial is designed to give a broad overview of ESD device technology, the many ways Circuit Designers protect against ESD, and the Failure Analysis (FA) techniques that are likely to be encountered in a report about ESD failures. This class is NOT intended to turn you into an ESD Protection Designer or an ESD Failure Analysis Engineer. It is meant for Program Managers; to give them background on what designers and FA engineers actually do, or for those users who want to have a broad, but not deep, understanding of those areas of the ESD world. After completing this tutorial you should be able to understand the basics of device ESD protection design and some of the trade-offs inherent in that process. You should also be familiar with some of the most commonly used failure analysis techniques that can help identify failing circuit components - in other words "what does a semiconductor manufacturer do with the units I return for failure analysis?" The topics covered include: the three most common ESD Models: HBM, CDM and MM; characteristics of ideal ESD protection; ESD failure analysis schemes; key characteristics of real ESD protection; failure analysis flow; failure analysis tools and their uses for ESD.

Tutorial EE: ESD Control for Extremely Sensitive Class 0 Devices

1:00 p.m. - 4:30 p.m.
Track Designation: FMEC
Albert Wallash, Hitachi Global Storage Technologies
Technical Level: Intermediate

This tutorial describes ESD control problems and practical solutions for handling all energy and voltage ESD sensitive devices. Special attention is given to solving ESD issues for the most ESD sensitive "Class 0" devices. Examples involving semiconductor devices, laser diodes, MEMs and magnetic recording devices are presented. All of the secrets on how to handle even a 1V CDM device are revealed! Both live and video demonstrations are used to clearly explain the problems and their solutions.

Tutorial FF: Sensitivity of MEMS to EOS/ESD Phenomena

1:00 p.m. - 2:30 p.m. NEW
Track Designation: DDT
Augusto Tazzoli, University of Padova
Technical Level: Basic

This tutorial addresses the important issues that EOS/ESD phenomena could cause on Micro Electro Mechanical Systems (MEMS). It will start with an overview on what MEMS are and the required theoretical background, up to showing simulated and experimental results, and practical design tips to improve device reliability. Theoretical basis will help to understand the main problems of micromachined devices: dielectric breakdown, charge trapping, stiction problems, etc. Electrostatically actuated MEMS for radio frequency applications will be analyzed in detail, but the results will be extended also to different devices with other actuation mechanisms (magnetic, thermal, piezo, etc…). Finite-Element-Method (FEM) and Electro-Magnetic (EM) simulations will be introduced through some examples with the aim of investigating more in detail the impact of EOS/ESD events on the device behavior. Experimental results will cover a significant part of the tutorial, in order to show real failures induced by EOS/ESD events, trying to remove misconceptions, and suggesting realistic protections from the design stage, up to the PCB assembling, always considering the problems and limitation typical of RF applications. Finally, the testing of MEMS devices will be analyzed, showing state-of-art setups ad-hoc developed for MEMS & ESD characterization, and analyzing the main differences from traditional solid-state devices testing.

Tutorial GG: Latch-up Physics and Design
3:00 p.m. - 4:30 p.m.
Certification: DD Track Designation: DDT
Steven H. Voldman, Intersil Corporation
Technical Level: Intermediate/Advanced

Latch-up continues to be of interest today in advanced CMOS, mixed signal (MS) CMOS, RF CMOS, BiCMOS, and BiCMOS silicon germanium. This latch-up tutorial will provide a discussion on device-level latch-up physics, latch-up metrics and design criteria, latch-up test structures, test methods, latch-up measurement techniques, device-level AZD simulation, and new latch-up issues. Both internal and external latch-up phenomena, as well as DC and transient latch-up will be addressed. Latch-up structures, guard ring physics, and characterization will be discussed in depth. This tutorial will provide examples of latch-up scaling issues to discuss latch-up device level simulation. Latch-up process solutions, such as heavily doped buried layers (HDBL) and triple wells will be shown. This tutorial will briefly discuss latch-up standards. It will end with a discussion on the state-of-the-art latch-up issues and characterization techniques and tools.

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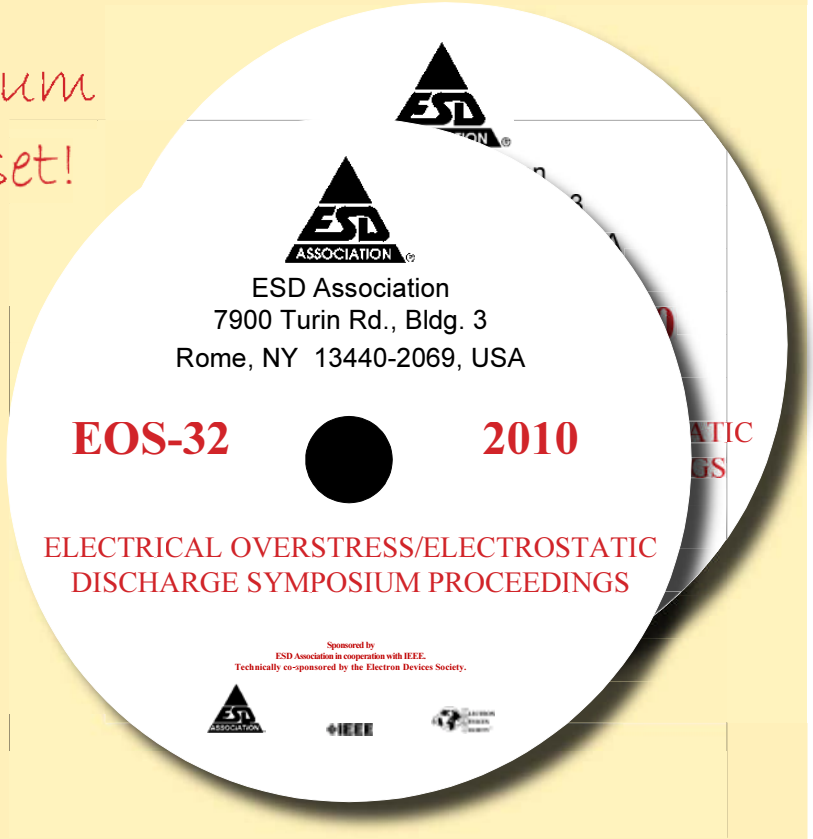

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TUESDAY 9:30 a.m. - 12:00 P.M. Parallel Sessions

Session 1A: On-Chip Physics Numerical Simulation and Modeling, Reliability Issues

Moderator: Guido Notermans, ST Ericsson

1A.1 A Scalable Verilog-A Modeling Method for ESD Devices

Weiying Li, Tina Tian, Linpeng Wei, Tommy Mao, Richard Wang, Chai Gill, Freescale Semiconductor

A novel Verilog-A modeling method is presented for ESD devices, which is simulator-independent, easy-to-implement and applicable to different device types. The behavior models are scalable with device dimensions and suitable for predictive ESD simulations. The method is validated by models of NMOS and Zener-triggered bipolar device with good silicon correlation.

1A.2 TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior

Johan Bourgeat, STMicroelectronics, CNRS; LAAS, Université de Toulouse; Christophe Entringer, Philippe Galy, Frank Jezequel, STMicroelelctronics; Marise Bafleur, CNRS; LAAS, Université de Toulouse

Silicon controlled rectifier (SCR) has a superior ESD performance in terms of power dissipation and saved area compared to the classical MOSFET. In this paper, we present 3D TCAD simulations of SCR in CMOS 32 nm node. This work focuses on the reduction of the parasitic overvoltage due to the SCR turn-on.

1A.3 A Novel Physical Model for the SCR ESD Protection Device

Alexandru Romanescu, ST Microelectronics, Institute of Microelectronics, Electromagnetism, and Photonics (IMEP-LAHC); Pascal Fonteneau, Charles-Alexandre Legrand, Jean-Robert Manouvrier, Helene Beckrich-Ros, ST Microelectronics; Philippe Ferrari, Jean-Daniel Arnould, Institute of Microelectronics, Electromagnetism and Photonics (IMEP-LAHC)

An SCR is one of the most efficient ESD protection devices. In order to improve the accuracy, convergence, scalability and the parameter extraction and support time, a new compact model was developed based on physical phenomena. The compact model was validated in a 40 nm CMOS technology.

1A.4 The Impact of Long-Duration Stress on ESD Clamps

Gianluca Boselli, Jonathan Brodsky, Hans Kunz, Akram Salman, Texas Instruments, Inc.

An analysis of long-duration TLP and DC stresses is performed on ESD clamps representative of the most commonly used protection strategies. A power-to-failure versus time-to-failure dependence valid across all the investigated clamps is shown. It is demonstrated that different ESD strategies have optimal performance only in a limited time domain.

1A.5 CDM Simulation Study of a System-In-Package

Vrashank Shukla, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

The work presents a static charge storage model for a stacked CSP and uses circuit simulations to investigate the voltage stress on the die-to-die interface circuits. Simulations show the impact of power net connections on the CDM reliability. An ESD protection scheme for the die-to-die interface circuits is proposed.

Session 1B: EOS and System Level ESD: Design and Simulation

Moderator: Alan Righter, Analog Devices, Inc.

1B.1 Triggering of Trasient Latch-up (TLU) by System Level ESD

Tilo Brodbeck, Wolfgang Stadler, Christian Baumann, Kai Esmark, Infineon Technologies AG

This paper investigates the influences of the temperature and the trigger parameters (width and rise time) on the threshold of transient latch-up (TLU). It is shown that an increase of the temperature is much more critical than transient trigger parameters. For high discharge currents which are typical for cable discharge events even very short trigger pulses can cause TLU.

1B.2 Measurement, Simulation and Reduction of EOS Damage by Electrical Fast Transients on AC Power

Al Wallash, Hitachi Global Storage Technologies; Vladimir Kraz, BestESD Technical Services

Electrical fast transients on AC power can result in electrical overstress (EOS) damage to an ESD sensitive device connected to the output of AC powered equipment. A methodology for measuring and simulating EFT transients is described. Techniques for reduction of the damaging transients are tested and analyzed.

1B.3 SPICE Simulation Methodology for System Level ESD Design

Lifang Lou, Charvaka Duvvury, Agha Jahanzeb, Jae Park, Texas Instruments, Inc.

A SPICE simulation methodology to design an isolation impedance network against the residual pulse from IEC 61000-4-2 stress for the system level ESD protection using the TLP data of transient voltage suppressors and IC interface pins is presented. A case study demonstrates the usage of this methodology.

1B.4 TLP Characterization for Testing System Level ESD Performance

Agha Jahanzeb, Lifang Lou, Charvaka Duvvury, Scott Morrison, Texas Instruments, Inc.

A practical approach to characterize system level ESD using TLP is presented. Good correlation to IEC 61000-4-2 test was obtained with biased and unbiased TLP. The biased TLP analysis was found to be a useful tool to improve the IEC performance.

1B.5 On-Chip System Level Protection of FM Antenna Pin

Guido Notermans, Dejan Maksimovic, Gerd Vermont, Michiel van Maasakkers, ST Ericsson; Fredrik Pusa, Catena Wireless Electronics; Theo Smedes, NXP Semiconductors

An on-chip protection against IEC 61000-4-2 discharges is presented. The protection level is tested by means of HMM stress. The failure signature is identified by means of TLP testing and physical failure analysis. A simple circuit model is presented which is able to predict the HMM failure level very well.

TUESDAY 1:00 P.M. - 3:30 P.M. Parallel Sessions

Session 2A: ESD Electronic Design Automation: Verification and Simulation

Moderator: Theo Smedes, NXP Semiconductor

2A.1 An ESD Design Automation Framework and Tool Flow for Nanoscale CMOS Technologies

Mujahid Muhammad, Robert Gauthier, Junjun Li, Ahmed Ginawi, James Montstream, Souvick Mitra, Kiran Chatty, Amol Joshi, Karen Henderson, Nicholas Palmer, Brian Hulse, IBM

We present a successfully implemented ESD design automation framework that evaluates and verifies the ESD protection methodology at all stages of a standard integrated circuit design flow. The tools used at each step of the flow and sample results, showing excellent correlation to hardware test data, are presented.

2A.2 Hierarchical Verification of Chip-Level ESD Design Rules

Ziyang Lu, Mentor Graphics Company; David Averill Bell, LSI Corporation

Verification of net-oriented ESD rules is rapidly becoming critical for nanometer design. To meet chip-level complexity and size challenges, a novel approach using topology-aware net types is developed to enable fast, hierarchical verification. This is applied to ESD design rules for power/ground interfaces and successfully adopted in production verification flows.

2A.3 An Automated ESD Verification Tool for Analog Design

Hans Kunz, Gianluca Boselli, Jonathan Brodsky, Texas Instruments, Inc.

There is an increasing need for automated ESD verification tools — especially for analog designs. This work describes the aspects of analog design that increase verification complexity and presents tool requirements based on these aspects. A new verification tool for analog design Is introduced.

2A.4 Predictive Full Circuit ESD Simulation and Analysis Using Extended ESD Compact Models: Methodology and Tool Implementation

Junjun Li, Robert Gauthier, Amol Joshi, Martin Lundberg, John Connor, Shunhua Chang, Souvick Mitra, Mujahid Muhammad, IBM

We present a new ESD compact modeling methodology using Verilog-A to enable predictive full circuit ESD simulation along with supporting hardware and failure analysis results. Also a new ESD tool (ESTEEM) to automate the ESD design simulation and optimization flow for circuit designers is described. Test results show excellent simulation to hardware data correlation.

2A.5 Cross Domain Protection Analysis and Verification Using Whole Chip ESD Simulation

Mototsugu Okushima, Tomohiro Kitayama, Susumu Kobayashi, Tetsuya Kato, Morihisa Hirata, NEC Electronics Corporation

A whole-chip simulation methodology of the full ESD paths, including the full-chip power and ground wiring network has been established and successfully demonstrated on products with several hundreds of pins. By checking voltage stress across cross domain circuits itself, the marginal ESD design window in sub-100 nm SoCs can be extended.

Session 2B: System Level ESD: Component Level ESD Correlation

Moderator: Leo G. Henry, ESD/TLP Consultants, LLC.

2B.1 Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation

Nicolas Monnereau, Fabrice Caignet, David Tremouilles, CNRS; LAAS, Université de Toulouse

In this paper we present a simulation methodology and measurements of a simple board, which shows the impact of an Integrated Circuit's (IC) external decoupling capacitance on ESD propagation. Resulting waveform is detailed and interactions between IC and components (including package, PCB and ESD protections) are highlighted.

2B.2 Impact of the Power Supply on the ESD System Level Robustness

Sandra Giraldo, LAAS CNRS, ON Semiconductor; Christophe Salamero, ON Semiconductor; Fabrice Caignet, LAAS CNRS

This work presents the case study of an audio amplifier. It shows that the discharge current path changes when the IC is stressed while being powered up. Simulations have been performed and compared to measurements to explain the IC failure under system ESD stress conditions.

2B.3 Effects of TVS Integration on System Level ESD Robustness

Wei Huang, David Pommeranke, Missouri University of Science and Technology (MST); Jeffrey Dunnihoo, NXP Semiconductors

Higher integration of Transient Voltage Suppression (TVS) functionality into ASIC I/O cells promises lower system costs. This work shows that as the ESD pulse is directed deeper into the system, migrating the TVS clamping function from the periphery of the system to a central ASIC may reduce the system's ESD robustness.

2B.4 Correlation between System Level and TLP Test Applied to Stand-Alone ESD Protections and Commercial Products

Patrice Besse, Jean-Philippe Laine, Alain Salles, Mike Baird, Freescale Semiconductor

This paper studies the correlation between the robustness at high current TLP and robustness during system level tests. The same relation has been confirmed between stand-alone ESD structures and commercial products using different technologies. A linear trend can be extracted depending on the R, C module of the gun.

2B.5 System to Component Level Correlation Factor

S. Thijs, D. Linten, P. Jansen, IMEC; M.Scholz, IMEC, Vrije Universiteit Brussels; C. Russ, W. Stadler, Infineon Technologies AG; D. LaFonteese, V. Vashchenko, A. Concannon, P. Hopper, National Semiconductor Corporation; M. Sawada, HANWA Electronics Ind. Co. Ltd.; G. Groeseneken, IMEC, Katholieke Universiteit Leuven

System to Component level Correlation Factors (SCCF) have been measured to range from 10 to 67% for various devices depending on physical mechanisms related to the device failure. Three main failure categories are defined: thermal failure of devices with either low or high holding voltage and failure due to voltage overshoots. In this paper it is shown how system level ESD robustness can be estimated based on available component level ESD results.

WEDNESDAY 8:00 A.M. - 9:40 A.M. Parallel Sessions

Session 3A: On-Chip Protection: Advanced CMOS - Analog, Digital and Latchup
Moderator: Steven Thijs, IMEC vzw

3A.1 On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8 kV Contact System Level
Bart Sorgeloos, Ilse Backers, Olivier Marichal, Bart Keppens, Sofics

For the design of on-chip ESD clamps against system level ESD stress, three main challenges exist: reaching a high failure current, ensuring latch up immunity, and limiting transient overshoots. Bearing these in mind, high system level ESD requirements should be within reach. A novel improved high holding current SCR is introduced, fulfilling all three requirements while drastically reducing silicon area.

3A.2 Pulsed Gate Dielectric Breakdown in a 32 nm Technology Under Different ESD Stress Configurations
Yang Yang, Dimitris E. Ioannou, George Mason University; Robert Gauthier, James Di Sarro, Junjun Li, Souvick Mitra, Kiran Chatty, Rahul Mishra, IBM

We report pulsed high-k gate dielectric breakdown in various configurations emulating ESD stress in real input/output circuits. The stress on the receiver is of a higher concern than on the driver due to different gate oxide areas under stress. Methods to improve the pad voltage tolerance with respect to gate oxide breakdown are proposed.

3A.3 Improved ESD Protection in Advanced FDSOI by SON/Bulk Co-integration
Thomas Benoist, ST Microelectronics, CEA-Leti Minatec, IMEP-LAHC; Claire Fenouillet-Beranger, Jean-Luc Huguenin, Stéphane Monfray, Pierre Perreau, ST Microelectronics, CEA-Leti Minatec; Nicolas Guitard, Philippe Galy, David Marin-Cudraz, ST Microelectronics; Christel Buj, Olivier Faynot, Francois Andrieu, CEA-Leti Minatec; Sorin Cristoloveanu, Pierre Gentil, IMEP-LAHC

We investigate the influence of different technological parameters on ESD robustness in advanced FDSOI devices. From TLP measurements, a comparison with other technologies enables us to evaluate the impact of ultra-thin film and buried oxide. A solution base on the co-integration of Silicon-On-Nothing/bulk is presented in order to make FDSOI ESD robust.

3A.4 Engineering Fully Silicided Large MOSFET Driver for Maximum It1 Performance
M.I. Natarajan, H. Jiang, H.K. Yap, G.W. Zhang, C. Wang, C. Cheng, P.R. Verma, GLOBALFOUNDRIES

Simultaneous optimization of LDD and anti-punch-through implant conditions for ESD performance of very large width silicided output driver nMOSFET without snapback mode of operation is reported. Physical mechanisms responsible for performance improvement and device sensitivity to pulse rise time, with little or no dependence on TLP pulse width, are detailed.

Session 3B: Factory and Materials: CDM Related Factory Issues
Moderator: Reinhold Gaertner, Infineon Technologies

3B.1 ESD Protection Program at Electronics Industry-Areas for Improvement
KP Yan, Reinhold Gaertner, CY Wong, Infineon Technologies

The ESD protection program set up in the electronics manufacturing facilities, especially in China region (evident but not limited to that area), appears to have common weaknesses. While a lot of ESD protection is implemented, it is often unclear if the right method is used at the right place. Multiple backup solutions ensure safe ESDS handling without big problems. With expected future limitations for on-chip ESD protection, it is necessary to enable correct assessment of the ESD risks for their production lines.

3B.2 CDM Damage Due to Automatic Handling Equipment
Sean Millar, Xilinx Ireland Ltd.; Jeremy Smallwood, Electrostatics Solutions, Ltd.

Charged Device Model (CDM) damage caused by Automatic Handling Equipment (AHE) to an FPGA product at an advanced test facility is reported. Careful study and characterization using a commercially available EMI monitoring system revealed significant static discharge events. They have been successfully eliminated through alternative AHE component selection.

3B.3 Measurements to Establish Process ESD Compatibility
Arnold Steinman, Electronics Workshop; Leo G. Henry, ESD/TLP Consulting, LLC; Marcos Hernandez, Thermo Fisher Scientific

There are no standards for establishing equipment or process capability to handle devices of known ESD sensitivity. Correlating verification methods with parameters of device testing is a first step. Measurements with a contacting high impedance voltmeter and ESD event detectors are compared to voltages and discharges of HBM and CDM testing.

3B.4 Comparison of Methods of Evaluation of Charge Dissipation From AHE Soak Boats
Jeremy Smallwood, Electrostatic Solutions, Ltd.; Sean Millar, Xilinx Ireland Ltd.

The charge dissipation of anodized surfaces of soak boats used in Automated Handling Equipment (AHE) was measured using standard and non-standard test methods. The results of tests showed considerable variation. It is concluded that some standard test methods do not give a representative measure of charge dissipation in this application.

WEDNESDAY 10:15 A.M. - 11:55 A.M. Parallel Sessions

Session 3A: On-Chip Protection: Advanced CMOS - Analog, Digital and Latchup - continued
Moderator: Steven Thijs, IMEC vzw

3A.5 Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies
Souvick Mitra, Robert Gauthier, Shunhua Chang, Junjun Li, Ralph Halbach, Chris Seguin, IBM

In advanced SOI technologies, the bottom gate voltage plays an important role in achieving the maximum Vt1 of the cascoded drivers. A comparable MOSFET and BJT current handling is needed to ensure maximum Vt1. The min and max Vt1 window for cascoded driver is shown to range between a single FET Vt1 and twice single FET Vt1.

3A.6 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering
Shuqing Cao, Robert Dutton, Stanford University; Jung-Hoon Chun, Eunji Choi, Sungkyunkwan University; Stephen Beebe, GLOBALFOUNDRIES

This work investigates the ESD robustness of stacked drivers in bulk and SOI technologies. The impact of stacked driver sizing and pre-driver connection is examined in detail using VF-TLP, TLP measurement and SPICE simulation. It is shown that proper pre-driver configuration can double Vt2 and improve It2 by 8 times.

Session 4A: On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 1)
Moderator: Lorenzo Cerati, STMicroelectronics

4A.1 A TLP-Based Characterization Method for Transient Gate Biasing of MOS Devices in High-Voltage Technologies
Joost Willemen, David Johnsson, Yiqun Cao, Matthias Stecher, Infineon Technologies

A method to characterize the dynamic behavior of high voltage MOS devices is presented. It utilizes TLP measurements to determine the MOS output characteristics with and without gate-coupling. It characterizes the gate-coupling that is defined by the ratio of the device capacitances. This is relevant for design of ESD circuits and compact modeling. Characterization of several HV devices illustrates the method.

4A.2 A New ESD Design Methodology for High Voltage DMOS Applications
Slavica Malobabic, Juin J. Liou, University of Central Florida; Javier A. Salcedo, Alan W. Righter, Jean-Jacques Hajjar, Analog Devices

A comprehensive methodology for synthesizing robust ESD performance in highly sensitive high voltage DMOS functional blocks is introduced. Optimizing high voltage output stage design for robust device- and system-level (IEC 61000-4-2) is assessed under 1-, 2-, 5-, 10- and 100-ns wide time frames of typical electrostatic discharge (ESD) stress models.

Session 4B: Factory and Materials: New Test Methods and Materials
Moderator: Rainer Pfeifle, Wolfgang Warmbier

4B.1 Actual Static Control Market Situation and How to Choose More Suitable ESD Flooring Systems for ESD Control Working Areas
Toshikazu Numaguchi, Sumitomo 3M Company LTD.

The ESD Association (ESDA) developed ANSI/ESD STM97.1 and 97.2 and also supported IEC 61340-4-5. These procedures are not well understood or utilized in the Asian market. Many electronics companies are handling miniaturized ESD susceptible devices (ESDS) at the working area. Many companies are developing an understanding of the ESD susceptibility voltage of their parts; but at the same time, defining and measuring the control level for personnel handling the parts often relies on electrical resistance measurements. This paper presents measurements of the personnel body voltage in actual factories handling miniaturized devices and shows the need to confirm not only resistance to ground but also body voltage generation when qualifying a floor and footwear grounding system for operators.

4B.2 Characterizing Slowly Dissipative Materials
Toni Viheriäkoski, Cascade Metrology; Matti Laajaniemi, Seppo Niemelä, Nokia Siemens Networks; Jukka Hillberg, IonPhasE Oy; Pasi Tamminen, NOKIA Corporation

Electrostatic properties of continuously grounded samples in a changing electrostatic field were studied. Response of the surface potential and transferred charge was simultaneously recorded while the sample was influenced by impulse of electrostatic field. An outcome of the study was a proposal for the new definition and characterization of slowly dissipative material.

4B.3 Neutralizing Current Sensor for AC Corona Ionizer
Kengou Yoshimizu, Masahiro Enokizono, Kazuo Okano, The Polytechnic University; Takashi Terashige, Hiroshima International University; Takashi Ikehata, Ibaraki University

New neutralizing current sensor for AC corona ionizer was proposed and investigated. The sensor can extract the neutralizing current by separating the static induction current, in spite that it is set close to the emitter. The neutralizing current has to be monitored to check the effect of an AC corona ionizer.

4B.4 Static Charge Induced Orientation of Liquid Crystals in LCD Panels
TaeYoung Kim, Korea University; DonSun Kim, JinHo Ju, LG Display; JongEun Kim, InsCon Tech. Co. Ltd.; Kwang S. Suh, Korea University, InsCon Tech., Co. Ltd.

Abnormal bright or dark spot images are classified into one of the LCD failures. We report here that this comes from the liquid crystal orientation, which is affected by the static charge-induced electric field. Based on the proposed mechanism, its prevention method are discussed in terms of materials and ionizers.

WEDNESDAY 2:30 P.M. - 4:10 P.M. Parallel Sessions

Session 5A: On-Chip Protection: Bipolar, SmartPower, RF, High Voltage (Part 2)
Moderator: Lorenzo Cerati, STMicroelectronics

5A.1 On the Dynamic Destruction of LDMOS Transistors Beyond Voltage Overshoots in High Voltage ESD
Yiqun Cao, Infineon Technologies, Technische Universität Dortmund; Ulrich Glaser, Joost Willemen, Matthias Stecher, Infineon Technologies; Stephan Frei, Technische Universität Dortmund

ESD protected LDMOS transistors shows sensitivity to voltage overshoots. ESD diode, NLDMOS and their combination are investigated in detail. The unique failure mode is identified as ongoing triggering of the parasitic bipolar transistor beyond a rise-time-dependent voltage overshoot of the ESD diode. Solutions for enhanced ESD protection are presented.

5A.2 Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays
V.A.Vashchenko, A. Strachan, D. LaFonteese, A. Concannon, P. Hopper, National Semiconductor Corporation; D. Linten, M. Scholz, S.Thijs, P. Jansen, G. Groeseneken, IMEC vzw

The self-protection capability (SPC) of integrated power arrays in ESD regimes has been studied for the case of integrated 100 V NLDMOS arrays in a BCD process. A new methodology for array comparison taking into account both gate coupling and avalanche current effects has been experimentally validated. Two orders of magnitude improvement of SPC has been demonstrated by implementation changes to array design.

5A.3 Study of DeMOS Power Arrays in ESD Operation Regimes
Blerina Aliaj, Juin J. Liou, University of Central Florida; Vladislav Vashchenko, Philipp Lindorfer, National Semiconductor Corp.; Andrew Tcherniaev, Maxim Ershov, Silicon Frontline

In this study, the self-protection capability of arrays dependent on layout design parameters is explored through the use of a new 2.5D simulation methodology and several topology elements improving array HBM robustness are identified. The physical effects responsible for local burnout are demonstrated.

5A.4 Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies
Akram A. Salman, Gianluca Boselli, Hans Kunz, Jonathan Brodsky, Texas Instruments, Inc.

This is a study of the parasitic NPN for high voltage BiCMOS technology. In this work, we investigate the spacing and edge effects using TLP and TCAD to identify the junction breakdown location. We also examine two solutions using highly doped base implant and deep trench isolation to reduce bipolar beta and mitigate parasitic NPN turn-on.

Session 5B: Factory and Materials: General Interest
Moderator: Jeremy Smallwood, Electrostatic Solutions, Ltd.

5B.1 Problematic Natural Gas Power Plant Pumping/Irrigation Station Lightning Protection Success Story
Douglas Miller, NNSA; Steven Hudson, Eddie Teague, Xcel

This paper documents activities of a design and engineering team that was created to develop and implement an effective solution to prevent damage from lightning. The lightning-caused damage was frequently occurring to an eastern New Mexico natural gas power plant grey water pumping/irrigation facility.

5B.2 ESD Stimulated Ignition of Metal Powders
Ervin Beloni, Edward L. Dreizin, New Jersey Institute of Technology

Interpretation of a conventional ESD ignition sensitivity test identifying minimum ignition energy for powders is difficult. It is proposed that more useful and readily measured quantitative indicators of the powder ignition sensitivity are burn time of the particles and the distance the burning particles travel at a given spark energy.

5B.3 Spacecraft Charging and an Instrument for its Monitoring Aboard the International Space Station
Boian Kirov, Katya Georgieva, Bulgarian Academy of Sciences; Vesselin Vassilev, Novorell Technologies

Electrostatic charging of satellites in space is a function of the spacecraft materials and various sources of charged particles. Novel instrumentation based on Langmuir probes designed and manufactured at STII-BAS, as a part of the Plasma Wave Complex (PWC) aboard the Russian segment of the International Space Station, monitors the surface charging of the station.

THURSDAY 8:00 A.M. - 9:40 A.M. Parallel Sessions

Session 6A: TLP, HBM, MM, CDM - Device Testing Testers, Methods and Correlation Issues (Part 1)
Moderators: Junjun Li, IBM; Melanie Etherton, Freescale Semiconductor, Inc.

6A.1 Pitfalls for CDM Calibration Procedures
T. Smedes, A. van IJzerloo, NXP Semiconductors; M. Polewski, NXP Semiconductors, Thales; J. L. Lefebvre, NXP Semiconductors, Presto Engineering; M. Dekker, MASER

A product qualification gave very different results for CDM testing between 3 labs. This paper describes the investigation into the root cause of these differences. The most relevant issues are the measurement bandwidth and the quality of the calibration modules. An improved procedure is proposed.

6A.2 Study of FI-CDM Discharge Waveform
RCJ Best Paper
Masanori Sawada, Taizo Shintani, HANWA Electronic Ind. Co., Ltd.

This paper describes the Field Induced CDM (FI-CDM) discharge waveform simulation methodology and results. Several standards are published for CDM leading to different measurement results. We simulate CDM waveforms for each standard explaining the difference in measured data and show the influence of parasitic effects on the discharge circuit in FI-CDM.

6A.3 Impact of Difference Between Discharging Methods on CDM Testing
Yasuyuki Morishita, Hiroyasu Ishizuka, Takayuki Hiraoka, Kenji Hashimoto, Nobuyuki Wakai, Shigetaka Kumashiro, MIRAI-Selete

We present significant difference between the relay and air discharging methods in CDM testing. The relay discharging method can give inaccurate CDM threshold due to a parasitic capacitance within the relay. It is shown that the air discharging is a better testing method to emulate CDM event under natural discharging condition.

6A.4 CDM2 - A New CDM Test Method for Improved Test Repeatability and Reproducibility
Robert Given, Marcos Hernandez, Tom Meuse, Thermo Fisher Scientific

Field Induced CDM (FI-CDM) test issues that have been substantiated by numerous industry sources are highlighted and addressed by a new test method called CDM2. This new method overcomes the majority of FI-CDM testing issues that negatively impact today's FI-CDM test repeatability and reproducibility. Most importantly, it eliminates the air discharge variable spark resistance. A new CDM standard test method is also proposed.

Session 6B: On-Chip ESD Failure Case Studies New Mechanisms, Phenomena and Troubleshooting
Moderator: Michael Stockinger, Freescale Semiconductor, Inc.

6B.1 Anomalous ESD Failures in NLDMOS during Reverse Recovery
Tetsuro Hirano, Mitsuo Hase, Takashi Ogura, Shuji Tanaka, Shuji Fujiwara, SANYO Semiconductor Co., Ltd.

Anomalous NLDMOS behavior under ESD stress is investigated. MM test results show failures at low stress voltage and local distribution of failure sites. TCAD simulations clarify that the reverse recovery current during the MM stress causes parasitic NPN turn-on and effectively lowers the trigger voltage (Vt1).

6B.2 ESD Protection Circuit Schemes for DDR3 DQ Drivers
Xiaofeng Fan, Michael Chaine, Micron Technology, Inc.

The high-speed interface of DQ pins in DDR3 DRAM requires special ESD considerations. During ESD characterization testing, high voltages from the power rail could pass through the pre-driver PMOSFET to reach the pull-down NMOSFET gate oxide. Special circuit design of the pre-driver circuit is required to eliminate this failure mechanism.

6B.3 CDM Effect on a 65 nm SOC LNA
Eugene R. Worley, Reza Jalilizeinali, Sreeker Dundigal, Evan Siansuri, Tony Chang, Vivek Mohan, Xiaonan Zhang, Qualcomm

A 65 nm SOC LNA showed unexpectedly low CDM performance. STI diode overshoot due to the very fast CDM pulse rise time was found to cause overstress and consequently rupture of the LNA's LV NFET amplifier. The solution included replacing STI with gated diodes and incorporating a secondary clamping scheme.

7B: Sub-Class 0 Devices, MR-Heads, MEMS
Moderator: Ted Dangelmayer, Dangelmayer Associates, LLC

7B.1 A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic Cures
Augusto Tazzoli, Marco Barbato, Vincenzo Ritrovato, Gaudenzio Meneghesso, University of Padova

The breakdown of 3D-micromachined devices with air-gap from 1.2 to 4.5 um was studied measuring the emitted electromagnetic field during the testing. The experimental evidence that short ESD events are not responsible for dielectric charging issues is also given. A simple, but effective, varistor based protection structure is explored.

THURSDAY 10:05 A.M. - 12:10 P.M. Parallel Sessions

Session 7A: TLP, HBM, MM, CDM - Device Testing Testers, Methods and Correlation Issues (Part 2)

Moderators: JunJun Li, IBM; Melanie Etherton, Freescale Semiconductor, Inc

7A.1 Investigation of Current Flow during Wafer-Level CDM Using Real-Time Probing
Nathan Jack, Vrashank Shukla, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

Using real-time voltage probing and circuit simulation, the stress induced by wafer-level CDM test methods is compared to that of package-level FI-CDM testers. It is shown that while wafer-level testers can replicate I/O failures, they may not replicate core failures because of differences in the induced current stress.

7A.2 A New Method to Evaluate Effectiveness of CDM ESD Protection
Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar, Andrew Olney, Analog Devices, Inc.; David Ellis, Juin J. Liou, University of Central Florida

A new methodology for evaluating the effectiveness of CDM protection is investigated. VF-TLP is used on structures composed of an ESD protection in parallel with a gate monitor, a MOS transistor or inverter. Shifts in Vth and Idd of the MOS monitor device are measured to continuously gauge the damage extent.

7A.3 HBM Tester Waveforms, Equivalent Circuits, and Socket Capacitance
Timothy J. Maloney, Intel Corporation

The Tektronix CT2 current probe is used to acquire more accurate Human Body Model waveforms with 0-Ohm and 500-Ohm tester loads, owing to the CT2's low-frequency performance. The integrals and centroids of these waveforms then readily yield precise values of tester circuit elements and effective socket capacitance.

7A.4 Unselected Pin Relay Capacitance HBM Tester Artifact
Scott Ward, Keith Burgess, Joe Schichl, Charvaka Duvvury, Peter Koeppen, Hans Kunz, Texas Instruments, Inc.; Evan Grund, Grund Technical Solutions, LLC

Pin relay capacitances degrade the rise-time of the ground path return current on HBM testers, causing failures on devices with transiently triggered ESD networks. Two pin HBM testing and TLP measurements have verified the failures as tester related. Updates to the HBM standards are needed to address this tester artifact.

7A.5 HBM Transient Safe Operating Area - A Case Study
M. Scholz, IMEC vzw, Vrije Universiteit; D. Linten, S. Thijs, IMEC vzw; D. LaFonteese, V. Vashchenko, A. Concannon, P. Hopper, National Semiconductor Corporation; M. Sawada, HANWA Electronics Ind. Co. Ltd.; G. Groeseneken, IMEC vzw, Katholieke Universiteit

The concept of transient safe operating area (TSOA) is introduced based on on-wafer HBM measurements with voltage and current waveform capturing using two case studies. The HBM TSOA parameters provide an easy way to give valuable insight in the device operation of ESD protection devices, circuits and their safe operating condition.

7B: Sub-Class 0 Devices, MR-Heads, MEMS - continued
Moderator: Ted Dangelmayer, Dangelmayer Associates, LLC

7B.2 Behavior of RF MEMS Switches Under ESD Stress
Sandeep Sangameswaran, Guido Groeseneken, Ingrid De Wolf, IMEC vzw, Katholieke Universiteit Leuven; Jeroen De Coster, Vladimir Cherman, Piotr Czarnecki, Dimitri Linten, Steven Thijs, IMEC vzw; Mirko Scholz, IMEC vzw, Vrije Universiteit Brussels

An integrated measurement setup is presented, which can do out-of-plane displacement measurements in MEMS during an ESD stress event. The setup enables ESD testing over different ambient pressure ranges and environmental conditions. Initial results on RF-MEMS capacitive switches are reported. The effect of ESD on the switch characteristics is investigated.

7B.3 Analysis of Dynamic Effects of Charge Injection Due to ESD in MEMS
William D. Greason, University of Western Ontario

A model is developed to analyze the effect of a leaky dielectric layer and air gap space charge on the frequency response of a capacitive MEMS structure. A straight line approximation technique is applied to estimate the transfer function for various input variables. Conditions for a no operation mode are assessed.

7B.4 ESD Events of Cabled GMR Sensors
Icko Eric Timothy Iben, IBM Corp.

ESD damage from cable discharge events (CDE) of magnetoresistive sensors is problematic in manufacturing magnetic tape drives. CDE initiated by touching the cable pads used to connect to external electronics represent one source. This paper addresses CDE from other contact points, including capacitive coupling to metal objects contacting the cable.

7B.5 A Study on the Application of On-Chip EOS/ESD Full-Protection Device for TMR Heads
Ray Nicanor M. Tag-at, Lloyd Henry Li, Hitachi Global Storage Technologies Philippines Corp.

The use of diodes for ESD/EOS protection of Class 0 tunneling magnetoresistive devices is measured experimentally and simulated with SPICE models. It is shown that normal operation of the device is unaffected by the diodes and the ESD failure level can be increased significantly.

7B.6 The Effect of ESD on the Performance of Magnetic Storage Drives
Icko Eric Timothy Iben, Gilda Lee, Stanley Czarnecki, Peter Golcher, Michelle Lam, IBM Corp.

GMR sensors used in the storage industry to read data written on magnetic media are easily damaged by ESD. While some ESD events completely destroy a sensor, others can leave the sensor in a partially damaged state (soft ESD). We study the effect of soft ESD damage on drive performance.

Workshops

Workshops Chair: Hans Kunz, *Texas Instruments, Inc., Dallas, TX*

You are invited to send your comments/questions in advance to the respective workshop moderators via e-mail or using the form at the ESDA web page (www.esda.org/workshops.htm).

Tuesday 4:00 p.m. - 5:30 p.m. (Parallel Sessions)

A1: Human Metal Model Testing

Moderator: Theo Smedes, *NXP Semiconductor*
e-mail: theo.smedes@nxp.com

This workshop is a forum for attendees to discuss their experiences implementing the ESDA Standard Practice on Human Metal Model (HMM). Topics include correlation between device-level HMM performance and system level performance, measurement techniques, and experiences with system-level disturb failures—which may not be predicted by device-level testing.

A2: ESD Control for Class 0 Devices

Moderator: Tim Iben, *IBM*
e-mail: iben@us.ibm.com

Manufacturers are constantly challenged to find ways to handle ESD sensitive devices in a cost effective manner. This workshop is an opportunity to discuss tool configuration, tool design best-practices, material selection and factory design—in the context of both effectiveness for ESD control and cost.

A3: ESD Verification Checks Leveraging Existing Commercial EDA Tools

Moderator: Robert Gauthier, *IBM*
e-mail: rgauthie@us.ibm.com

There is an industry-wide desire to involve EDA vendors in the creating new tools for ESD design verification. An interesting pre-cursor to new tool development is the use of existing tools in novel ways to solve new applications. This workshop is a forum for attendees to share ways that they have exploited existing EDA tools to solve ESD verification problems—perhaps giving EDA vendors new insights into how existing tools can be leveraged—and with what limitations

Tuesday 6:00 p.m. – 7:30 p.m. (Parallel Sessions)

B1: Sources of EOS Damage and Characterization Techniques for Determining EOS Robustness

Moderator: Chai Gill, *Freescale Semiconductor, Inc.*
e-mail: rynd90@freescale.com

This workshop will provide attendees an opportunity to discuss mechanisms that cause EOS damage. The workshop will focus on EOS mechanisms other than latch-up, exploring EOS mechanisms for which robustness requirements and testing standards are either limited in scope or non-existent (e.g., reverse power, over-voltage, and hot-plug). Attendees are encouraged to share techniques they have developed for characterizing EOS robustness.

B2: Board-Level Solutions to System-Level ESD Design

Moderator: Harald Gossner, *Infineon*
e-mail: harald.gossner@infineon.com

There has been a great deal of discussion in the ESD community regarding increasing requirements for full integration of system-level ESD protection on-chip. While this continues to be an important topic, there is also a need to discuss board-level solutions (components and techniques) to address the system level ESD problem. This workshop is an opportunity to discuss board-level protection strategies that do not require full integration of system-level ESD cells onto the IC. Co-design strategies where the board-level solution works in concert with the existing (non-system-level) on-chip protection will also be discussed.

B3: Common ESD Audit Issues

Moderator: Ted Dangelmayer, *Dangelmayer Associates, LLC*
e-mail: ted@dangelmayer.com

ESD auditing is the driving force behind a solid ESD control program. This workshop is an opportunity to discuss common ESD audit findings and their proper solution with industry experts.

Workshops Chair: Hans Kunz, *Texas Instruments, Inc., Dallas, TX*

You are invited to send your comments/questions in advance to the respective workshop moderators via e-mail or using the form at the ESDA web page (www.esda.org/workshops.htm).

Wednesday 5:00 p.m. – 6:30 p.m. (Parallel Sessions)

C1: Equipment Grounding Issues

Moderator: TBD
e-mail:

This workshop will focus on ESD Control requirements for automated handling equipment. Common problems/solutions to equipment grounding in the factory will be discussed, including test methods for determining the effectiveness of a grounding strategy.

C2: Challenging Pin Applications in Analog Design

Moderator: Gianluca Boselli, *Texas Instruments, Inc.*
e-mail: g-boselli@ti.com

Product requirements often challenge state-of-the-art technologies and ESD design techniques. While there has been good discussion regarding high-speed digital and high frequency RF topics, there are numerous power analog, precision analog, high-voltage, and negative voltage requirements which present daily challenges to ESD Engineers across the industry. This workshop is an opportunity to share difficult applications and to discuss potential solutions.

C3: ESD Challenges Due to Package Scaling and Integration

Moderator: Elyse Rosenbaum, *University of Illinois at Urbana-Champaign*
e-mail: elyse@illinois.edu

Larger packages with higher pin counts and smaller pin pitch are increasingly complicating ESD testing. Further, increased integration of multiple ICs and even passive components into a single package is increasing ESD complexity—often pushing the need for ESD design verification up to the package integration level. ESD engineers are now being challenged to design ESD protection networks which cross IC boundaries—this workshop is a forum for discussing this evolving aspect of ESD design and testing.

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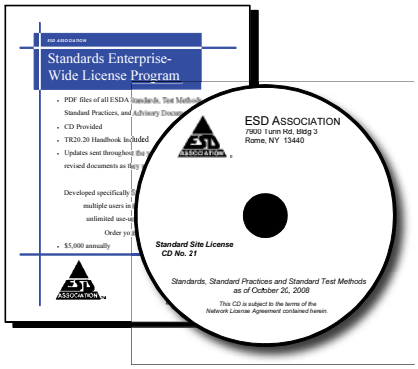

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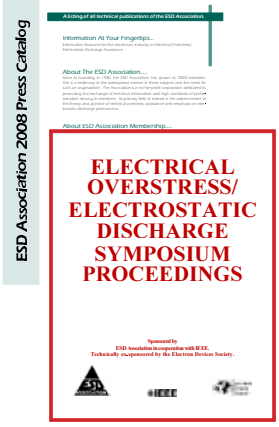

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A lunch service will be avalable in the exhibit hall on Tuesday, for anyone wishing to purchase lunch while visiting the Exhibits.

Tuesday's hours have been extended to allow attendees the opportunity to visit the hall during the workshop break!

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Registration - page 1

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2 Tutorial & Seminar Registration

Check each session attending, one session per time slot.

SUNDAY, OCTOBER 3 & MONDAY, OCTOBER 4

☐ S20.20 8:00 a.m. - 5:00 p.m. ESD Program Development and Assessment (PrM)

SUNDAY, OCTOBER 3

☐ A 8:30 a.m. - 4:30 p.m. ESD Basics for the Program Manager (PrM)
☐ B 8:30 a.m. - 4:30 p.m. ESD On-Chip Protection in Advanced Technologies (DD)
☐ C 8:30 a.m. - 4:30 p.m. ESD Protection and I/O Design
☐ D 8:30 a.m. - 12:00 p.m. System Level ESD/EMI: Principles, Design Troubleshooting, and Demonstrations
☐ E 8:30 a.m. - 12:00 a.m. Triboelectrification - Theory and Applications
☐ F 8:30 a.m. - 10:00 a.m. Perfect ESD Storm
☐ G 10:30 a.m. - 12:00 p.m. Circuit Modeling and Simulation for On-Chip Protection (DD)
☐ H 1:00 p.m. - 4:30 p.m. System Level ESD/EMI: Testing to IEC and Other Standards (PrM) (DD)
☐ I 1:00 p.m. - 4:30 p.m. Use of the Digital Sampling Oscilloscope for ESD Measurements
☐ J 1:00 p.m. - 4:30 p.m. ESD Ignition & Fires

MONDAY, OCTOBER 4

☐ K 8:30 a.m. - 4:30 p.m. How To's of In-Plant ESD Survey and Evaluation Measurements (PrM)
☐ L 8:30 a.m. - 12:00 p.m. Ionization Issues and Answers for the Program Manager (PrM)
☐ M 8:30 a.m. - 12:00 p.m. SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits (DD)
☐ N 8:30 a.m. - 12:00 p.m. On-Chip ESD Protection in RF Technologies (DD)
☐ O 8:30 a.m. - 12:00 p.m. Troubleshooting On-Chip ESD Failures (DD)

MONDAY, OCTOBER 4 Continued

☐ P 8:30 a.m. -10:00 a.m. Design and Application of VF-TLP and cc-TLP Systems Targeted for CDM
☐ Q 10:30 a.m. - 12:00 p.m. Advanced Topics in TLP & VF-TLP Testing
☐ R 1:00 p.m. - 4:30 p.m. Packaging Principles for the Program Manager (PrM)
☐ S 1:00 p.m. - 4:30 p.m. Device Testing-Component Level: HBM, CDM, MM, and TLP (DD)
☐ T 1:00 p.m. - 4:30 p.m. Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design (DD)
☐ U 1:00 p.m. - 2:30 p.m. Charged Device Model Phenomena and Design (DD)
☐ V 1:00 p.m. - 2:30 p.m. HMM Basics: Standard Practice, Testing Procedures and Round Robin Study
☐ W 3:00 p.m. - 4:30 p.m. CDM ESD Circuit Simulation Methods for ESD Design and Failure Debug
☐ X 3:00 p.m. - 4:30 p.m. TLP Measurements: Parametric Analyzer for ESD On-Chip Protection (DD)

THURSDAY, OCTOBER 7

☐ Y 8:30 a.m. - 12:00 p.m. Cleanroom Considerations for the Program Manager (PrM)
☐ Z 8:30 a.m. - 12:00 p.m. EOS/ESD Failure Models and Mechanisms (DD)
☐ AA 8:30 a.m. - 12:00 p.m. Electrostatic Calculations for the Program Manager and the ESD Engineer (PrM)
☐ BB 8:30 a.m. - 12:00 p.m. Automated Handling and Processes
☐ CC 1:00 p.m. - 4:30 p.m. ESD Standards Overview for the Program Manager (PrM)
☐ DD 1:00 p.m. - 4:30 p.m Device Technology and Failure Analysis Overview (PrM)
☐ EE 1:00 p.m. - 4:30 p.m ESD Control for Extremely Sensitive Class 0 Devices
☐ FF 1:00 p.m. - 2:30 p.m. Sensitivity of MEMS to EOS/ESD Phenomena
☐ GG 3:00 p.m. - 4:30 p.m. Latch-up Physics and Design (DD)

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3 Fees: Please check appropriate boxes

Symposium	Early Registration Fees On or Before Aug 9, 2010	Registration Fees After Aug 9, 2010
(Includes technical sessions, workshops, and exhibits)		
☐ ESD Association Members	$545	$745
☐ Non-Members	$645	$745
Tutorials - Member Prices		
☐ Sunday (Full Day)	$495	$695
☐ Sunday (Half Day)	$295	$495
☐ Monday (Full Day)	$495	$695
☐ Thursday (Full Day)	$495	$695
☐ Thursday (Half Day)	$295	$495
Tutorials - Non-Member Prices		
☐ Sunday (Full Day)	$595	$695
☐ Sunday (Half Day)	$395	$495
☐ Monday (Full Day)	$595	$695
☐ Thursday (Full Day)	$595	$695
☐ Thursday (Half Day)	$395	$495

Student Fees 50% discount for full-time students. Proof of enrollment required. Student fees apply only to Symposium or Tutorial Registration and do not apply to Bundled Fees or Seminar Fees.

	Early Registration Fees On or Before Aug 9, 2010	Registration Fees After Aug 9, 2010
Bundled Fees		
(Symposium plus Sun., Mon. and Thurs., full days of tutorials)		
☐ ESDA Members	$1,730	$2,410
☐ Non-Member	$2,070	$2,410
Bundle Fee does not include S20.20 Seminar		

ESD Program Development and Assessment (Sun & Mon)		
(ANSI/ESD S20.20 Seminar)		
(Attendance limited to first 30 registrants)		
☐ ESD Members	$1,495	$1,695
☐ Non-Members	$1,595	$1,695
This seminar is NOT included in Bundle Fee		

Symposium Proceedings

☐ Printed copies $150 each. **Must be ordered and paid for by Aug 9** to receive on site. (Each paid registrant receives one copy of the Proceedings on a flash drive. See page 1 for details.)

Register online at esda.org/onlineregistrations.html

4 Payment • Company purchase orders not accepted.

☐ **Check** (Make payable to ESD Association)

TOTAL ENCLOSED $ _____

Type (circle): Visa® Master Card ® AMEX® Discover®

Credit Card # _____

Expiration Date: _____ **Security Code (CVV):** _____

Print Name on Card: _____

Include payment with this form. Mail form and payment to: ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069, USA, Tel: 315-339-6937, Fax: 315-339-6793. Students must include proof of full-time enrollment to obtain student fees. Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve, travelers checks payable in U.S. dollars, and credit cards (Visa®, MasterCard®, AMEX®, and Discover®) will be accepted. Pick up registration materials at the Registration Desk when you arrive. **Cancellation & refund requests** will be honored if received in writing no later than Aug 9, 2010.

Hotel

All reservations must be received by September 3, 2010

John Ascuaga's Nugget Resort
1100 Nugget Avenue,
Sparks, Nevada 89431
Phone: 800-648-1177
Fax: 775-356-4198
www.januggetsecure.com/jump/1171

Room Rates for Symposium:
$85 in the West Tower and $99 in the East Tower*

Complimentary wireless internet will be provided for 1 person in each attendee room.

*East tower rooms recently remodeled

Name: _____ Company: _____

Address: _____ City: _____

State/Province: _____ Zip/Postal Code: _____ Country: _____

Accommodations Requested
☐ Single/Double ☐ Accommodations under the Americans with Disabilities Act

Room rates shown do not include applicable taxes and surcharges.

Arrival Date: _____ Departure Date: _____

List all persons who will be sharing accommodations

_____ _____

_____ _____

Reservation Guarantee

Name on Card: _____ Card Type (circle) Visa® Mastercard® AMEX® Discover®

Credit Card #: _____ Expiration Date: _____

Cardholder's Signature: _____

Deposits and Reservations: A one night's room and applicable taxes deposit or a guarantee with a major credit card is required to secure a reservation. When reserving your room, in all instances, identify yourself the group name Electrostatic Discharge Association (ESDA).

Cancellation of reservation must be made at least three days prior to arrival to receive a refund on deposit.

Wireless Internet Service: Complementary wireless internet will be provided for one person in attendee room.

Resort Fee: $5.00 per room, per night Resort Fee. This fee includes unlimited use of our Atrium Pool, Health Club, Valet Parking, Covered Garage Parking, Airport Shuttle, and Full-service Concierge.

ESD Association
7900 Turin Road, Building 3
Rome, NY 13440

Next Year's Symposium

2011 EOS/ESD SYMPOSIUM AND EXHIBITS

September 11-16
Disneyland Hotel,
Anaheim, CA
USA

The International Technical Forum on Electrical Overstress and Electrostatic Discharge

Sponsored by the ESD Association in cooperation with the IEEE.
Technically co-sponsored by the Electron Devices Society.

5/10/10